Design Automation of ΔΣ Switched Capacitor Modulators using SPICE and MATLAB

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Abstract: Concerning the fact that the design of contemporary integrated circuits (IC) is practically impossible without using sophisticated Electronic Design Automation (EDA) software, this paper gives some interesting thoughts and considerations about that issue. As technology processes advances on year basis consequently EDA industry is forced to follow this trend as well. This, on the other hand, requires IC designer to frequently and efficiently accommodate to new working environments. Authors of this paper suggest a method for high level circuit analysis that is based on using common (open source or low cost) circuit simulators but precise and fast enough to meet requirements imposed by demanding mixed-signal blocks. The paper demonstrates the proposed EDA procedure on an example of second order ΔΣ modulator design. It illustrates considerable simulation time saving which is more than welcome in a world of analogue and mixed-signal design.

Keywords: Electronic Design Automation, Modelling, ΔΣ modulation; Analogue and mixed-signal circuitry.

1 Introduction

Integrated circuits design depends on EDA tools and skills of the designer to use them. Leading EDA software development companies such as Cadence®, Mentor Graphics® and Synopsis® invests a lot of financial and intellectual resources to provide qualitative and efficient software environments. These design tools implement complex algorithms such as equation solvers, floor planers, routers etc. The problem is particularly pronounced in tools for the design of complex mixed-signal circuits. System level design of these circuits needs high-level modelling approach. It is supported by Hardware Description Languages (HDL) on the EDA tools market such as Veriolog-AMS, Verilog-A, VHDL-AMS, System Verilog, SystemC etc. All of them provide many high-end capabilities and practically define a standard in high-level modelling. The complete IC design flow requires different levels of model abstraction for different design phases. High-level models are simplified and verification is relatively fast and efficient. Physical design level involves more complex

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models that take into account second order effects. This increases accuracy at the expense of reduced efficiency.

The appropriate EDA environment should save design time but still preserve dissent amount of accuracy. There are two aspects that EDA should support. First, Top Down methodology, where it supposes to help circuit designers to extract key design parameters bringing them closer to the physical realization. And second, Bottom Up methodology, when finished designs have to be characterized to provide as accurate as possible model which will serve in system-level design. Concerning this second aspect, remarkable results for Continuous Time (CT) class of circuitry is accomplished in [1]. Nice thing about CT circuits is that the designer does not have any hard constraint when choosing type of the simulation to use. In other words one can use all from the simulator set i.e. operation point (quiescent), transient, DC and AC. Of course the best insight into circuit operation gives transient analysis but it consumes large amount of time.

Different problem arises regarding Discrete-Time (DT) analogue and mixed-signal blocks. The most popular realization of this type of circuits in CMOS processes is based on Switched Capacitor (SC) circuits.

High level models are well known and suitable for system level design. However, at lower levels only transient analysis (TR) is available to designers. Unfortunately it is the most time consuming. Therefore there is a real need for methods capable to make it faster with minimal loss of accuracy.

Aside to the complexity and excellent design automation possibilities the modern EDA tools are usually very expensive. Besides design libraries are covered with very expensive licensing policy. Consequently, they are not affordable to smaller design teams and companies.

This paper proposes a new procedure to automate the design process of SC circuits using low cost or free CAD tools. The method is based on SPICE platform in conjunction with appropriate MATLAB scripts. Namely it uses free version of SPICE optimized for switched regulators provided by Linear Technology Inc [2]. MATLAB platform is chosen for design automation because it is widespread in engineering community and it certainly drops in to the spectrum of common engineering skills. Practically even free version of MATLAB (or its free derivatives such as FreeMat or Octave) can provide quite respective signal processing, data management and data presentation capabilities. All this makes these two software tools attractive ingredients for building an inexpensive, custom EDA platform.

The paper describes this tool and its possibilities in five sections. The next section defines the problem of SC circuits design taking as an example the second order $\Delta\Sigma$ CIFF (Cascade of Integrators Feed-Forward) architecture. The third section explains the proposed EDA procedure and strategy for its

realization. The adopted target parameters for figure of merit are covered as well. The subsequent section presents simulation results which illustrate functionality of the prototyped EDA platform. Finally, findings and further development directions of the proposed EDA platform are sublimated in the conclusion.

2 Basics of Second Order ΔΣ CIFF Modulator

The problems related to SC circuits design will be revealed using the second order ΔΣ CIFF modulator as an example. More about system level analyses and simulation of this architecture in ADC applications can be found in [3]. Physical realization of second order ΔΣ architectures is well described in [4]. Since detailed schematic of fully differential topology of the modulator is reported in [5] only conceptual illustration of the schematic is presented in Fig. 1.
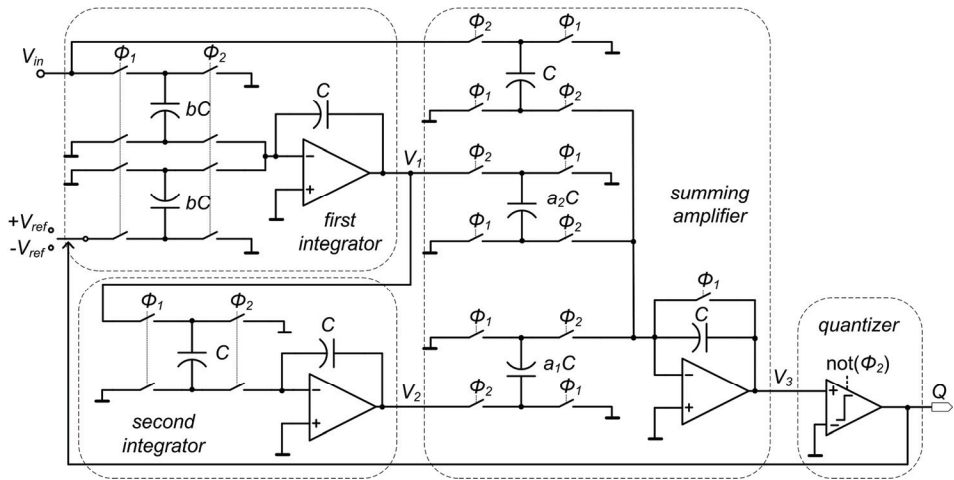

Fig. 1 – *Simplified schematic of second order ΔΣ CIFF modulator.*

Fig. 1 represents single sided topology with common mode voltage at ground potential.

According to the general theory of SC circuits the second order ΔΣ CIFF modulator operates in two non-overlapped clock phases, Φ_1 and Φ_2 at frequency f_s. In phase Φ_1 charges proportional to input voltages of the first and the second SC integrators are stored at input capacitors. Simultaneously capacitors in the summing amplifier are discharged. During Φ_2 phase the accumulated charge is transferred to feedback capacitors of integrators, defining voltages V_1 and V_2. The summing amplifier adds them to the input voltage V_{in} and produces V_3. Since phase Φ_2 defines a new value at output, the output voltage has to be stable

throughout that period. Consequently it is clocked with not(Φ_2) delivering plus or minus V_{ref} at the input of the first integrator.

Circuit in Fig. 1 provides second order, Z-domain, High Pass (HP) noise transfer function (NTF) given with (1)

$$NTF(z) = \frac{z^2 - 2z + 1}{(z - p_1)(z - p_2)}. \qquad (1)$$

The aim of this example is to obtain signal-to-noise ratio (SNR) of at least 80dB. According to [5] p_1 and p_2 should have values $0.3819 \pm j0.3004$. Oversampling ratio (OSR), maximum base bandwidth (BW), and full-scale voltage (V_{FS}) of this modulator are estimated to 256, 24 kHz and 0.8 V respectively [3, 5]. **Table 1** summarizes basic circuit parameters that meet the aforementioned requirements [3].

Table 1
Parameters for modulator model.

Parameter	Description	Value
a_1	coefficient	11/3
a_2	coefficient	4/3
b	coefficient	1/3
V_{ref}	reference voltage	0.6 V
f_s	sampling frequency ($\Phi_{1/2}$ clock)	12.6 MHz

The value of C determines the tolerable value of kT/C noise. It is good if C is as large as possible. However, in practice, it is limited by physical dimensions for given technology. For this project it is accepted that the in-band contribution of kT/C noise at room temperature ($T = 300$ K) is $[(4\,kT/C)/(2OSR)]^{1/2} = 4.5\ \mu V$. Therefore the smallest capacitance in the circuit is set to 1.7 pF.

3   EDA Procedure for Design of Second Order ΔΣ CIFF Modulator

As one can see from Fig. 1 there are a lot of switches operating at high frequency. In addition to abrupt changes caused by switching, effects like kT/C noise and clock feed through arise, as well. Besides, the parasitic effects of other components, such as Operational Transconductance Amplifier (OTA), affect the output. All of these effects define error budget of the modulator. Therefore it is good to know boundaries of circuit parameters before transistor level design. Their determination needs algorithm in three steps:
1. Set parameter values,

2. Run simulation (time domain),
3. Analyse results and make decision.

Every step is a specific challenge for designer.

Setting initial parameter values must be based on sound knowledge of the characteristics of the selected target design technology. Otherwise the process will turn to hazardous lucky-guess principle that wastes a lot of time and money.

Although functionality of the circuit can be easily lexically described TR analysis is not a trivial task. Every switching change local time constants at particular nodes and, consequently, modifies the circuit configuration. This produces very severe and time consuming simulation condition. The stepwise response to switching behaviour may easily lead to divergence problems. Hence special care has to be devoted to setting simulator options and initial conditions, primarily for capacitors.

Analysis of the obtained result is a separate problem. Namely, output of the quantizer produces discrete values form the set $\{0, V_{DD}\}$, i.e. $\{0, 1\}$ in digital domain, at every $1/f_s$ s. The only way to get insight into circuit behaviour is FFT analysis. According to [7] it requires at least (64 x OSR) points in time. In the particular case for $OSR = 256$ it gives 16384 points.

Finally, the decision about acceptable circuit behaviour is based on data arising from FFT analysis. Namely an additional effort is needed to calculate figure of merit for design expressed in terms of SNR and/or $SFDR$ (*Spurious Free Dynamic Range*) from the obtained output signal spectrum.

Practically, the parameter extraction process requires a lot of file management work which is usually done manually. For example, in order to extract parameters for the built-in OTA one has to begin with initial, nearly ideal, model parameters, to run a time domain simulation, process output data i.e. calculate FFT, to plot spectrum, and evaluate SNR and $SFDR$. Then the decision has to be made which model parameter to loosen in order to make it realizable and repeat the procedure. Finally a corner analysis should check whether the requirements are met for all model parameters.

Defining e.g. at least five OTA model parameters with two possible sweep values for each of them involves ten time domain simulations where one parameter is swept and the other four are held constant. All this produce a large amount of data to be processed. It is clear that this represent tedious work prone to errors. Therefore the designer needs a help. This paper promotes a software aid that is based on using low-cost and/or open source engineering tools. Fig. 2 illustrates the proposed solution for automation of the described procedure.

The whole process of automation has been entrusted to MATLAB computing engine (MCE). It is based on a script that can be roughly divided in two main sub-blocks of code.
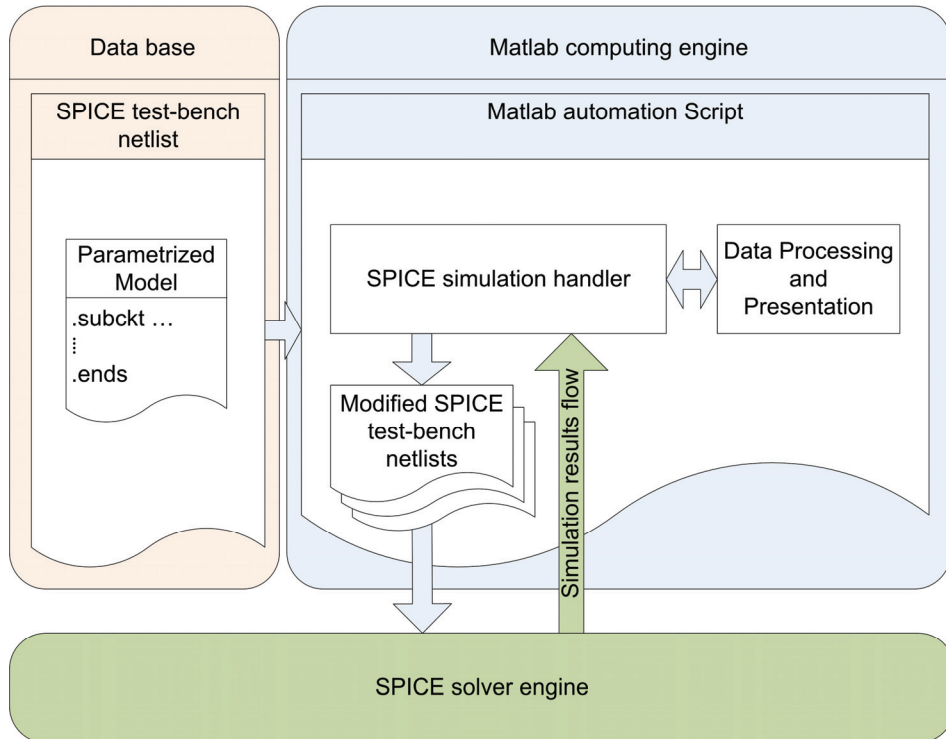

Fig. 2 – *Illustrative block diagram of the proposed EDA tool.*

The first is responsible for running and monitoring SPICE engine, and simulation results data management. Consequently it is named *SPICE Simulation Handler* (SSH). The second, called *Data Processing and Presentation* (DPP), serves as post-simulation data processor and presenter. It controls all substantially important data processing e.g. parsing, FFT computation, and *SNR* estimation.

SSH reads SPICE netlist with built-in $\Delta\Sigma$ model and generates multiple modified versions for given range of model parameter values. SPICE solver engine (SSE) simulates the modified test-bench netlists sequentially one by one. SSH detects end of simulation, collects obtained data and, if necessary, run the simulation again. This is the most delicate block of the script code because it must successfully handle with tools connection point.

It should be emphasized that this is an early version of software that serves to confirm the automation process idea. Therefore optimization algorithm for

OTA's design parameters is not implemented yet. It is up to the designer to order which parameter to be processed next. Anyway, engineer is released of data management labour that was the primary goal of this work. The next step performs DPP. Its role will be explained on a real example in the subsequent section.

4   Simulation Results

In the following illustrative example the goal is to design ΔΣ CIFF modulator (Fig. 1) that would have *SNR* > 80 dB, as previously mentioned, and *SFDR* > 90 dB relative to full scale within baseband limited to 24 kHz.

Transient analysis is the crucial part of the design process. In order to obtain elements for error budget calculation at an early design phase one needs a robust time domain macromodel of the modulator. It should consist of SPICE primitives and subcircuits. Bearing this in mind the authors developed an original SPICE macromodel. It includes Operational Transconductance Amplifier (OTA) model that takes into account effects of finite DC gain; finite bandwidth; slew rate; tail current of differential par and noise sources.

The initial parameters for OTA SPICE macromodel are given in the **Table 2**.

Table 2
Initial parameters for OTA model.

Parameter	Description	Value
A_{DC}	DC gain	80 dB
slr	Slew rate	1.26 V/ns
f_{gbw}	Gain bandwidth product	1.26 GHz
v_n	Max. offset noise amplitude	6.1 μV
v_{nktc}	Max. offset noise amplitude	6.1 μV
I_0	Max. diff. par tail current	100 μA
V_{DD}	Power supply voltage	0.6 V
V_{CM}	Common mode voltage	0.6V

Initial values for parameters A_{DC}, slr, f_{gbw}, I_0, V_{CM} are nearly ideal. A value for offset noise amplitude, v_n, corresponds to 1/2 of the least significant bit voltage value, v_{lsb}. In this case for V_{FS} = 0.8V and 16 bit resolution v_{lsb} is

12.2 μV. Since value for *C* is chosen high enough to reduce *kT*/*C* noise an additional noise source is introduced to model high noise conditions. The value for this source is set to $v_{lsb}/2$, as well.

Firstly, ideal second order CIFF architecture is simulated using MATLAB script. Ideal model of the architecture is realized purely mathematically using difference equations with no second order effects. This serves for booth initial system level circuit verification and setup of adequate FFT analysis parameters.

It is very important to choose appropriate frequency of the test signal and the fitting windowing function. This choice is so critical that can make or break spectral estimation of the output signal. Too few data points give poor spectrum image of the considered signal making SNR and SFDR estimate inaccurate. On the other hand to many data points lead to irrationally long simulation and data post processing time. Therefore trade-off between this two aspects hast to be made. Choosing proper windowing function with sharp high frequency attenuation in its spectrum will significantly reduce number of data points and unavoidable noise leakage. Also coherent sampling criteria should be appreciated as well. This means that input test frequency should fall exactly at integer multiple of the FFT frequency bin in order to reduce spectral leakage. In this case minimum number of data points is 2^{14} i.e. 16384 as previously determined in section 3. This number is sourly good enough for fast estimation of the spectrum. However for more detailed picture higher frequency resolution i.e. larger number of data points such as 2^{18} gives better result. The reader is advised to look in [6] for the details about spectral estimation. **Table 3** summarizes the adopted parameters for FFT analysis.

Table 3
FFT analysis parameters.

Parameter	Description	Value
N	FFT length	2^{18}
f_{in}	Test signal frequency	3.84 kHz
V_{in}	Test signal amplitude	0.4 V
Window	Windowing function	Hann

Fig. 3 illustrates output signal spectrum of the ideal second order CIFF architecture with no second order non-idealities. The upper plot in Fig. 3 shows spectrum with linear frequency scale up to the base band limit of 24 kHz. The lower plot represents the same spectrum in log-log scale where the noise-floor

slope of +40 dB/dec in out of band is evident. In both cases ordinate axis are represented in decibels relative to full scale to emphasize that input is fed with V_{FS}. The obtained value at f_{in} bin is –7.959 dBFS which corresponds to 0.4 V amplitude of input signal. For this, ideal case *SNR* is 91.34dBFS, and *SFDR* in the baseband is 108.48 dBFS. These results reflect ideal circuit behaviour.

Now the developed EDA script is used to estimate circuit behavior with included real parameter values of the built-in OTA. Two crucial parameters were considered: slew rate and DC gain.
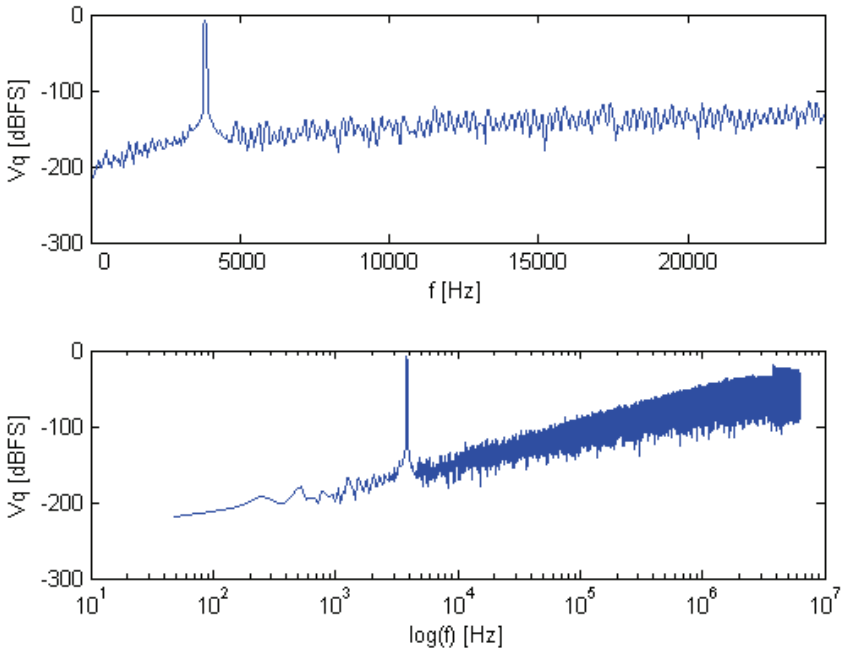

Fig. 3 – *FFT spectrum of the ideal second order CIFF output.*

Fig. 4 shows results obtained using behavioral SPICE model of the ΔΣ structure including OTA with gainbadwidth, f_{gbw} = 126 MHz, and slew rate $slr = k_{slr}$ (12.6 V/μs), where $k_{slr} \in \{100, 10, 1, 0.1\}$. All other parameters are left as in **Table 2**.

The parametric analysis in Fig. 4 reveals that for slr = 1.26 V/ns and slr = 126 V/μs the modulator satisfies the design specifications. For slr = 12.6 V/μs there is a rise of the odd order harmonics (3rd at 11.52 kHz and 5th at 19.2 kHz). In this case *SFDR* is limited at third harmonic to 58.4 dBs. For the lowest slewrate value, slr = 1.26 V/μs, function of the circuit is significantly distorted with high noise floor and the odd harmonic presence.

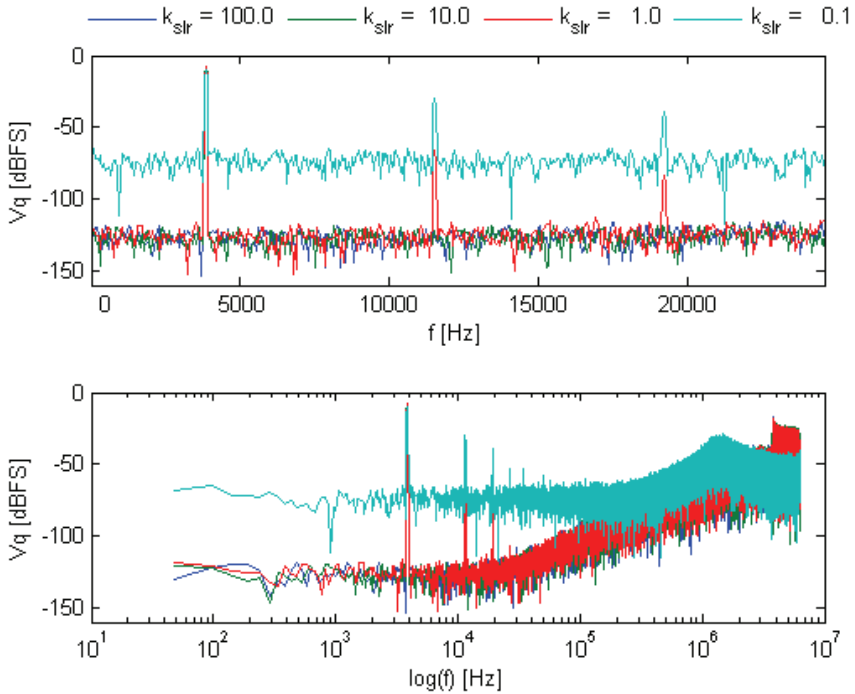**Fig. 4 –** *FFT spectrum of the second order CIFF output for limite gainbandwidth and a set of slew rate values.*

Table 4 summarizes *SNR* and *SFDR* values in dependence of *slr*. It is important to stress that *slr* value of 12.6 V/µs is not acceptable even *SNR* satisfies 80 dB constraint. This is because *SFDR* is drastically reduced to 58.4 dB which is over 30 dB beyond the required 90 dBs.

Therefore *slr* ≥ 126 V/µs is adopted as the minimal acceptable value.

Table 4
SNR and SFDR for various slew rate values.

slr [V/µs]	SNR [dBFS]	SFDR [dBFS]
1260	90.52	106.60
126	91.29	107.80
12.6	89.56	58.40
1.26	36.48	20.35

Real DC gain of OTA (A_{DC}) is the second parameter that will be examined. Besides the value used for the case of idealized amplifier A_{DC} = 80 dB, the

modulator response was checked for 60 dB, 40 dB and 20 dB. In all cases slew rate and gain bandwidth product were fixed to 126 V/µs and 126 MHz, respectively.

Fig. 5 shows influence of DC gain reduction to the modulator output signal spectrum. **Table 5** summarizes the corresponding *SNR* and *SFDR* values. The obtained results show that even rather low $A_{DC} = 40$ dB provides acceptable *SNR* and *SFDR* values. Only extremely low $A_{DC} = 20$ dB significantly deteriorates circuit characteristics. Here odd harmonics again becomes dominant. Nevertheless relatively high gain is always desirable in such circuits hence DC gain of $A_{DC} = 60$ dB was accepted as an achievable value.
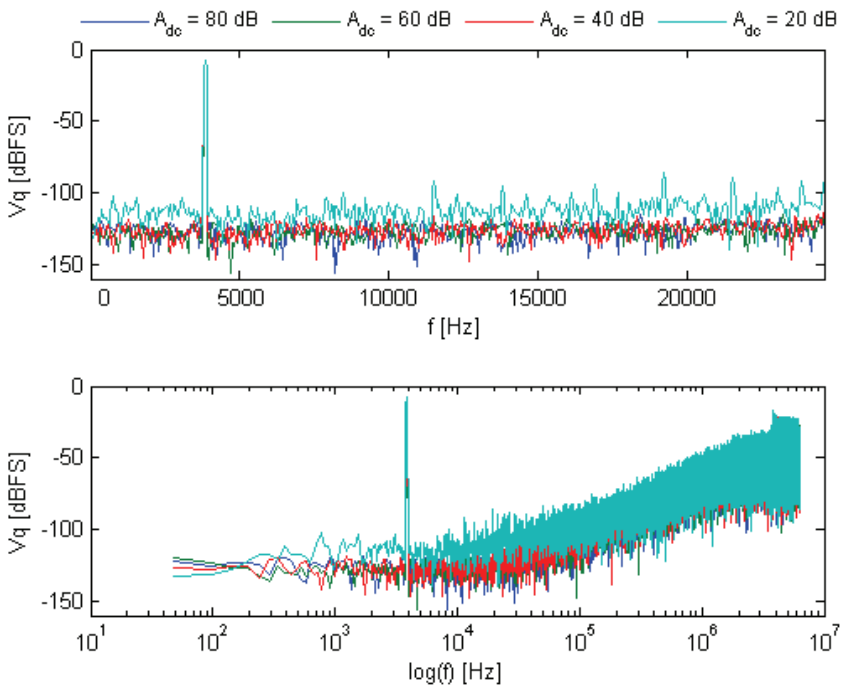

Fig. 5 – *FFT spectrum of the second order CIFF output for limited gainbandwidth and a set of slew rate values.*

The proposed EDA platform with SPICE macro-model spared a lot of data management work and resulted with considerable time saving. Total simulation time in the case of four OTA parameter values i.e. four transient simulations using 2^{18} data records is about eight hours. In comparison, one transistor level transient simulation of such circuit lasts several days on the same hardware platform.

Table 5
SNR and SFDR for various DC gain values.

A_{DC} [dB]	SNR [dBFS]	SFDR [dBFS]
80	90.98	107.19
60	91.38	106.67
40	90.06	105.63
20	73.54	78.05

Experiments showed that usable FFT results can also be obtained with 2^{14} points. This reduces SPICE simulation time and aforementioned set of simulations is provided for half an hour. Therefore the proposed procedure will gain tremendous time savings if one starts design with large parameter increments and TR analysis in fewer points (2^{14}) until define rough parameter boundaries. Then the design can proceed with smaller increments in more points. Namely the designer is able to fit the resolution according to the particular design phase in two dimensions: parameter increments and time steps.

5 Conclusion

The prime goal of this paper was to present an EDA tool that helps discrete-time circuit designers to detect boundary values of real parameters for built-in blocks. The idea was to postpone classical transistor level transient analysis of switched circuits until the very late design phase. Therefore it is based on macromodels with included constrains imposed by real parameter values. Challenges and aspects of EDA software development were commented first. Problems concerning simulation of complex mixed-signal blocks were emphasized as well. The paper considered a second order CIFF ΔΣ modulator as an example. The goal was to determine basic parameters values of built-in OTA that will keep the design features within the desired specification.

Standard procedure requires repetitive TR analysis for different parameter values and post-processing FFT. This time consuming task was accelerated by script programming. The software solution is based on SPICE simulator and MATLAB. The fundamental components of the tool are *SPICE Simulation Handler* and *Data Processing and Presentation*. The first manipulate with SPICE netlist, performs analysis and provides data for the second. *Data Processing and Presentation* executes FFT and delivers graphical output. OTA Simulation results confirmed model validity and justified the proposed EDA procedure. Simulation time saving of one order of magnitude was obtained. Moreover, the designer is able to trade simulation time for accuracy according to the current requests.

It is proved that decent EDA tool can be developed using low cost or free software platforms. This prototype version of software could be further improved in both flexibility and appearance.

6   Acknowledgement

7   References

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