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Optimizing DC and RF Characteristics of Pseudomorphic AlGaN/InGaN/GaN HEMT for GHz Application

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Abstract: This paper presents a design and in-depth analysis of DC and RF characteristics of Pseudomorphic AlGaN/InGaN/GaN High Electron Mobility Transistor (HEMT) for microwave application. Experimental data from an AlGaN/InGaN/GaN HEMT is used to validate the simulation results based on the I_d-V_g curve and transconductance, demonstrating their close agreement. Subsequently, the study focuses on investigating the impact of varying device parameters namely Indium (In) proportion of InGaN, gate length, source to gate length (L_{sg}) and gate to drain length (L_{gd}), and InGaN layer thickness. Sequential analysis has been done for various device parameters as a function of frequency. The results indicate that the device exhibits optimal performance when configured with an Indium (In) proportion of 0.15, a gate length of 0.40μm, an InGaN layer thickness of 2 nm and L_{sg} and L_{gd} of 1.15 μm, and 1.15 μm respectively shows f_t 15.36 GHz and f_{max} 37 GHz which is almost more than twice of the original calibrated device. These findings provide valuable insights for designing devices with enhanced performance.

Keywords: Electron Devices – III-V, HEMT, Gallium nitride, Semiconductors III-V, InGaN.

1 Introduction

HEMTs were developed in response to the demand for high frequency, low noise, and high-power density applications [1]. These HEMT devices feature heterojunctions formed by the combination of two distinct bandgap materials, effectively confining electrons in a quantum well to reduce impurity scattering [2]. Among the various HEMT devices, the AlGaN/GaN HEMT stands out as an exceptional device that has attracted significant research interest in recent years [3−6]. GaN has reached saturation electron velocities of 2.5 X10^7cm/s and a band gap of 3.39 eV. These exceptional material qualities make it an ideal material for

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high-powered devices [7, 8]. GaN also benefits from the two-dimensional electron gas (2DEG) generated at the AlGaN/GaN heterojunction contact, which has a high electron density and mobility. GaN HEMTs are ideally suited for high-power, high-frequency applications, and typically have a relatively high S_{21} magnitude which is useful for indicating strong power amplification and efficient signal transmission in radio frequency (RF) and microwave applications. [9, 10]. GaN HEMTs are capable of operating at extremely high frequencies, have satisfactory performance, and possess a high breakdown strength and electron saturation velocity [11, 12]. GaN provides a strong piezoelectric polarisation, which facilitates the accumulation of a large number of carriers at the AlGaN/GaN interface. Despite these benefits, electron confinement is compromised by the leakage of electrons into the buffer layer, resulting in suboptimal performance [13]. A new kind of HEMT structure was given to overcome this limitation and further enhance the performance of AlGaN/GaN HEMTs. This involves incorporating a low band gap InGaN layer at the AlGaN/GaN heterointerface [14]. This novel addition is anticipated to address the issue of leakage current from the buffer and significantly enhance the confinement of the two-dimensional electron gas (2DEG). Consequently, it is anticipated that the overall performance of the HEMT will be notably enhanced [15]. InGaN (Indium Gallium Nitride) is a material that has been explored for use as the channel layer in HEMT because it has high electron mobility and high saturation velocity, which are desirable characteristics for high-frequency and high-power applications [16]. When used as the channel layer in a HEMT, the InGaN layer is typically grown on top of a GaN (Gallium Nitride) layer. The InGaN layer forms a channel of two-dimensional electron gas (2DEG). At the AlGaN/InGaN heterointerface, there is a positive polarization charge, while at the InGaN/GaN heterointerface, a negative polarization charge is formed. The process of polarization is thoroughly explained in reference [17]. The InGaN layer is typically grown using MOCVD or MBE techniques. Adding an InGaN layer to a device can introduce a few challenges, which need to be carefully considered during the device design and fabrication process. The layer's composition and thickness can be tailored to optimize the device's electrical properties, such as the threshold voltage and transconductance [18 – 20]. So basically, in this paper we have designed and analyzed the dependency of DC and RF characteristics on various parameters including the thickness of the channel layer and x value in $In_xGa_{1-x}N$ (In proportion).

The whole paper is divided into 4 sections and 4 subsections. Section 1 gives the Introduction about the HEMT and background info on the material used in the device and their significance, Section 2 which is device design and calibration along with methodology, focuses on building the device on Silvaco Atlas and discussing the methods and models and various required data for calibration. Later Section 3 is Results and Discussions which is further categorized into four

subsections: a) optimizing by changing in proportion, b) optimizing by changing Gate length, c) optimizing by changing the thickness of the channel layer d) optimizing by modulating source to gate length (L_{sg}) and gate to drain length (L_{gd}), and e) comparison of the calibrated and optimized design. At last Section 4 is the conclusion which discusses the findings of the paper and its significance and leaves the reader with a clear understanding of the importance and implications of the paper along with its future scope.

2 Design and Calibration of Device and Methodology

GaN/AlGaN HEMTs were chosen due to their high electron mobility, broad bandgap, and high breakdown voltage. Moreover, GaN has a high thermal conductivity and permits high-frequency operation. Fig. 1 compares some of GaN's most important electronic properties to those of other semiconductors [7, 8]. These characteristics make GaN/AlGaN HEMTs well-suited for applications requiring high power and high frequency. In AlGaN/GaN HEMT structures, the 2DEG is positioned in the GaN channel layer immediately above the GaN buffer layer. This structure, however, lacks a sharp potential barrier at the rear of the 2DEG channel, resulting in poor carrier confinement and increased buffer leakage current. In addition, the electrons in the 2DEG channel may leak into the buffer, reducing their mobility. The replacement of the GaN channel with lattice-matched or strained materials with a lower conduction band than the GaN buffer is one strategy for addressing this issue as shown in Fig. 2 [20].

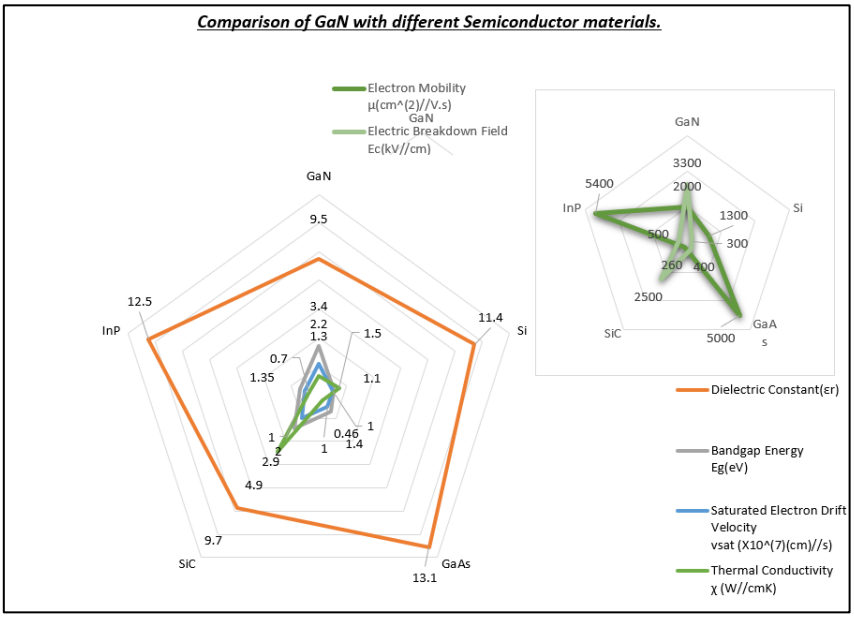


Fig. 1 – *Comparison of GaN with different Semiconductor materials* [7,8].

A potential alternative is the use of an InGaN layer, which provides enhanced carrier confinement by forming a barrier on one side and a buffer on the other. This method has been investigated as a way to improve the efficacy of HEMTs. InGaN has a different lattice constant than some of the commonly used substrates such as sapphire, silicon carbide, and silicon. This can result in lattice mismatch, which can cause defects and strain in the crystal structure. This can affect the electronic and optical properties of the material and degrade the device's performance.

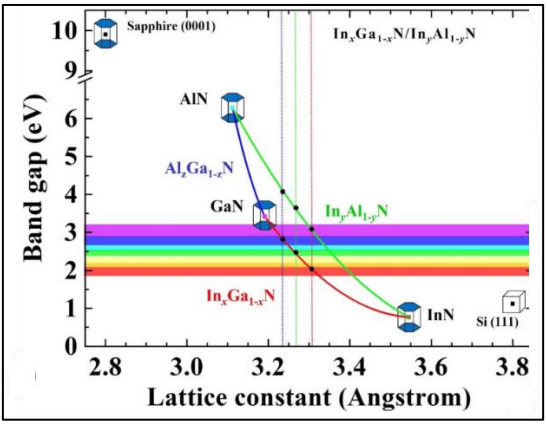


Fig. 2 –*The graph plots the III-nitride band-gap energy against the lattice constants. The lattice-matched points of the* $InxGa_{1-x}N/InyAl_{1-y}N$ *quantum wells for blue, green, and red-light emissions, respectively, are shown by the blue, green, and red dashed lines* [21].

To overcome this, it is important to carefully control the growth conditions and doping levels during the fabrication process of the InGaN layer and carefully decide the composition of In so that its performance is optimal [21].

TCAD allows us to perform virtual experiments and simulations before fabricating the actual device, reducing development time and costs. So, we designed the device on the Silvaco Atlas [22] using the parameters shown in **Table 1**. Starting with a SiC substrate, an AlN relaxation layer (1.5nm), Undoped GaN buffer layer (1.5 μm), an InGaN channel of 5nm is sandwiched between the buffer and undoped AlGaN spacer layer(5nm), doped AlGaN supply layer of 20nm is applied over spacer layer, 5nm GaN cap layer used to protect the supply layer from oxidation. Thereafter contacts were defined. The composition of In in InGaN was 0.10 and the percentage of Al in AlGaN (25.3%). In the preliminary phases, comprehensive simulations were conducted to calibrate the AlGaN/InGaN/GaN HEMT based on the experimental data previously reported by Khan et al. in their study [23]. Fig. 3a shows the cross-section view of the experimental device and Fig. 3b shows small signal equivalent circuit diagram. In Fig. 3, as well as in other figures um represents μm.

Simulation tools are important for optimizing designs without fabrication. In this paper, simulation-based design, analysis, and optimization of AlGaN/InGaN/GaN pHEMT has been done. Source and drain form Ohmic contacts with undoped GaN layer. The metal gate forms a Schottky contact with the supply layer of the un-doped wideband gap AlGaN layer by etching the cap layer. The Indium content in the $In_{.10}Ga_{0.90}N$ channel and the conduction band discontinuity at the interface mainly determine the two-dimensional electron gas density and mobility. Physics-based models used for these simulations are fermi srh fldmob pch. elec and GANSAT.N as the mobility model is used. In order to avoid the convergence problem Newton method is used. To calibrate the device based on an experimental paper we started by estimating initial parameter values from the paper or previous knowledge. Then performed a parameter sweep in the simulation software, varying the values within a range. Then Simulated the device using different parameter combinations and compared the results with the experimental data.

Table 1
Device Structural Parameters [23].

Parameters	**Values**
Undoped AlGaN (spacer layer)	5nm
Undoped GaN (buffer layer)	1.5μm
Substrate SiC	400μm
AlN Nucleation (relaxation layer)	1.5nm
GaN (Cap layer)	5nm
AlGaN (supply layer)	20nm
InGaN (channel layer)	5nm
In proportion	0.10
Work function	5.1
Gate length	0.50μm
Gate width	100μm
Length between source and gate	1μm
Length between gate and drain	2.75μm
Doping (algan layer)	1.14e13 cm^{-3}
Interface charge	$10e^{11}$
Length of source	0.25μm
Length of drain	0.25μm

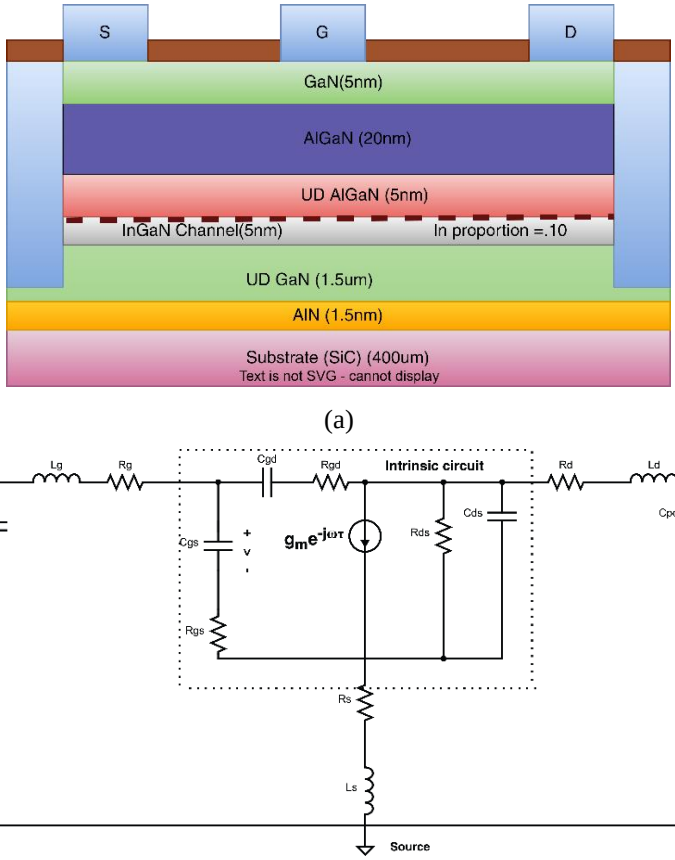


Fig. 3 – (a) *Schematic cross-sectional view of* AlGaN/InGaN/GaN *HEMT as proposed in* [23]*;* (b) *Small-signal equivalent circuit for HEMT* [24].

After the rigorous and exhaustive process of modulating the parameters, the device mentioned in the literature [23] is designed and calibrated. The author thoroughly understood this device's composition and geometry, and they applied that knowledge to fit the I_d-V_g curve to the experimental data. To achieve a precise fit of the I_d-V_g (current-voltage) data, the model was calibrated to experimental data by adjusting and fine-tuning various parameters. Fig. 4 at $V_d = 15\text{V}$ depicts both the simulation results and the experimental device I_d-V_g curve under standard room temperature conditions. Additionally, the transconductance curve (g_m) as a function of V_{gs} is presented in the same context. On analyzing the simulated and experimental curves, it is evident that there is a significant level of concurrence between the two, suggesting that the device has been suitably calibrated. Fig. 5 shows I_d-V_g curve at different gate voltages viz, 0V, 1V and 2V.

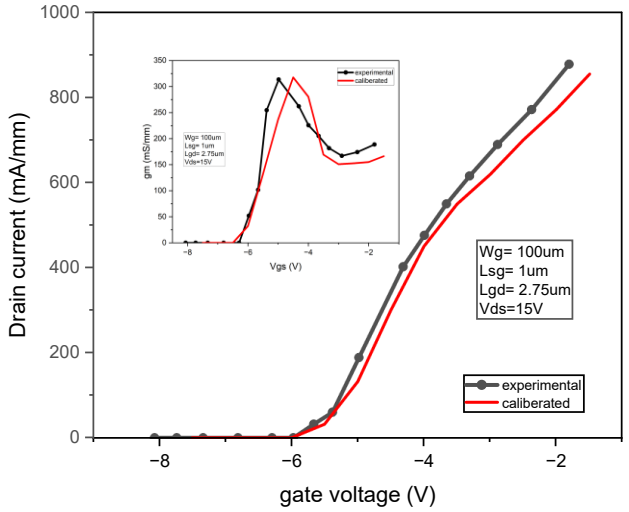


Fig. 4 – *Comparison between the experimental data* [23] *and the calibrated simulation model for the Transfer Characteristic at* V_d=15V *and default room temperature conditions.*

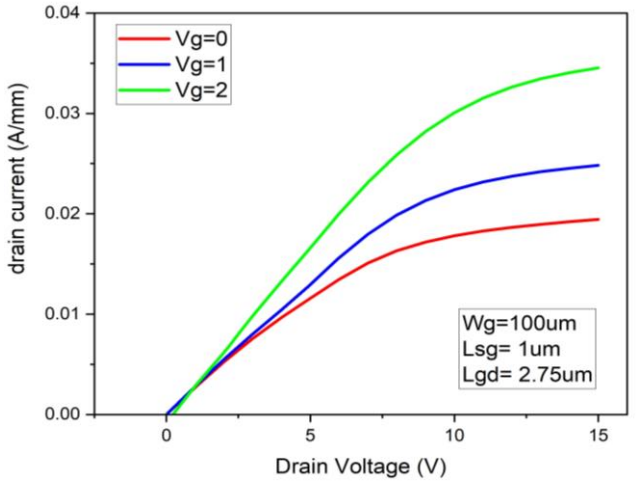


Fig. 5 – *Output characteristic of* I_d-V_d *at different* V_g.

3 Results and Discussions

This particular section is divided into four subsections, focusing on the design and analysis of four crucial parameters of the device through parameter tuning to report the best possible results. In the first subsection, we have optimized the In proportion in InGaN. Different proportions of indium were

studied, and their effects on the DC and RF performances were thoroughly analyzed. The objective was to determine the "In" proportion that produced the highest performance. In the second subsection, the design and analysis of the gate length parameter are dealt with. The influence of various gate lengths on the performance of the device is evaluated. By systematically varying the length of the gate and conducting thorough simulations, the optimal length of the gate is determined. The focus of the third subparagraph is the L_{sg} and L_{gd}. Extensive simulations were conducted to determine the effect of varying L_{sg} and L_{gd} keeping gate length (L_g) constant on the device's properties. Through careful analysis of the trade-offs between performance and a variety of other factors, the optimum L_{sg} and L_{gd} is determined. Lastly, the fourth subsection focuses on the InGaN layer's thickness. The impact of different InGaN layer thicknesses on the device's DC and RF performance is investigated. The simulations enabled a thorough evaluation of the impact of varying thicknesses, leading to the determination of the optimal InGaN layer thickness.

Throughout these subsections, the parameters were systematically tuned and analyzed with the end goal of identifying the optimal parameter combination that led to the highest device performance. The results obtained are reported, providing valuable insights for the design and optimization of the AlGaN/InGaN/GaN HEMT for improved DC and RF characteristics.

3.1 Optimization by changing x proportion of $In_xGa_{1-x}N$

We varied the proportion on $In_xGa_{1-x}N$ to check the change in DC and RF characterization.

Fig. 6 illustrates the observed trend of the DC characteristics as the proportion of $In_xGa_{1-x}N$ (referred to as "*x*") is increased. The graphs indicate that as the value of x increases, the drain current exhibits a notable increase, with a significant change observed between *x* values of 0.10 and 0.15. For *x* values beyond 0.15, the change in drain current becomes relatively minimal.

Subsequently, when characterizing RF devices, the cut-off frequency f_t, and the maximum frequency of oscillation $f_{\max}$, are regarded as the most crucial figures of merit. f_t and $f_{\max}$ are dependent on V_d and as the drain to source voltage increases f_t and $f_{\max}$ also increase up to a certain point [25]. f_t and $f_{\max}$ is described by the following expression from (1) to (4):

$$f_t = \frac{g_m}{2\pi(C_{GS}+C_{GD})(1+g_{ds}(R_S+R_D))+C_{GD}g_m(R_S+R_D)}, \qquad (1)$$

where the source and drain resistances are R_S and R_D, respectively, and the gate-source capacitance is C_{GS} and the drain-source capacitance is C_{GD}.

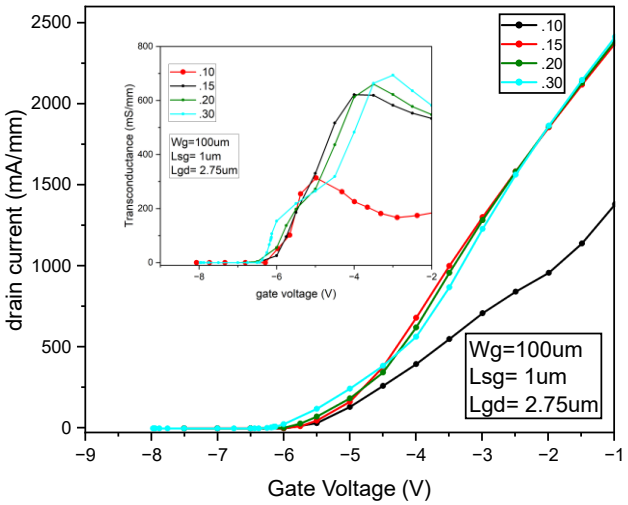


Fig. 6 – *DC transfer characteristics for changing proportions of x in* $In_xGa_{1-x}N$ *(*V_d = 15V*).*

If we ignore the impact of the parasitic resistances, the previous formula can be made simpler:

$$f_t \approx \frac{g_m}{2\pi C_{gg}}, \tag{2}$$

where g_m is transconductance and C_{gg} is gate capacitance.

$$f_{\max} = \frac{f_t}{4\sqrt{\frac{g_{DS}(R_G + R_D + R_S) + (2R_G + R_D + R_S)}{C_{GD} f_t}}}, \tag{3}$$

where C_{GD} represents gate-drain capacitance while R_G represents gate resistance. Even though increasing the f_t will increase $f_{\max}$, lowering other parasitics (such as capacitances and resistances) is also seen to increase $f_{\max}$. The parasitic resistances can be removed from the previous equation to make it simpler.

$$f_{\max} \approx \sqrt{\frac{\pi f_t}{8 C_{GD} R_G}}. \tag{4}$$

f_t and $f_{\max}$ can also be directly calculated using the equations or can be reported directly by analyzing the Tony plot and could be extracted from current gain vs frequency and unilateral power gain vs frequency graph. The frequency at which the transistor's incremental short-circuit current gain (H_{21}) falls to 1 is known as f_t. It is an important predictor of the high-speed performance of transistors [25].

Unilateral power gain is defined as the maximum power gain that can be obtained from the two-port after it has been made unilateral with the help of a lossless and reciprocal embedding network [26]. A transistor is said to be unilateral if the signal/power bounced back from the output to the source is equal to 0. This occurs if the reverse transmission coefficient, S_{12}, or the reverse transducer power gain, $|S_{12}|^2$ is equal to 0 [26].

Formula for unilateral power gain is given by (5):

$$U = \frac{|S_{21}/S_{12} - 1|^2}{2k|S_{21}/S_{12}| - 2\mathrm{Re}[S_{21}/S_{12}]}, \tag{5}$$

where k is

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{21}S_{12}|^2}{2|S_{12}S_{21}|} \tag{6}$$

For the derivation of unilateral power gain reference [26, 27] could be referred. The frequency when the transistor's U drops to 1 is known as $f_{\max}$ and f_t is the frequency where current gain becomes equal to 1 (0 dB) as mentioned below with (7) and (8) [28, 29]. Plotting these two parameters versus frequency yields the cutoff frequency f_t and $f_{\max}$ and is extracted from the graphs shown in Figs. 7a and b.

$$U(f)\big|_{f=f_{\max}} = 1 = 0\,\mathrm{dB}, \tag{7}$$

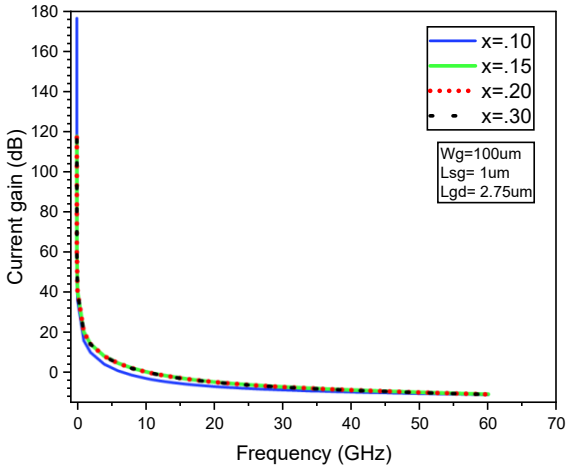
$$|H_{21}(f)|^2\Big|_{f=f_t} = 1 = 0\,\mathrm{dB}. \tag{8}$$

Referring to **Table 2** it is evident that the InGaN channel layer with 0.15 In Proportion comparatively shows higher cut-off frequency and max frequency of oscillation. The original pHEMT with indium proportion 0.10 shows $f_t = 6.49\,\mathrm{GHz}$ and $f_{\max} = 17\,\mathrm{GHz}$.

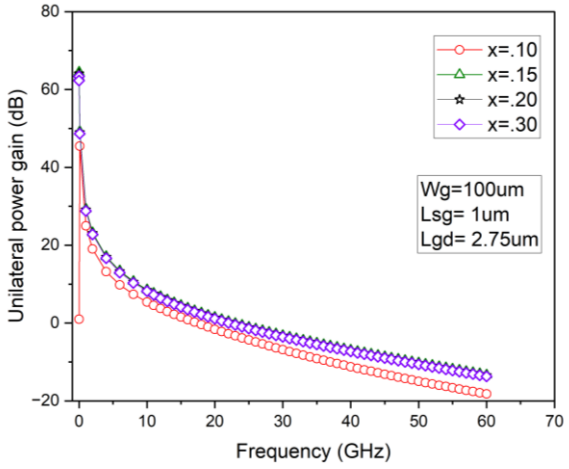
Table 2

Comparison of f_t and $f_{\max}$ at different proportions.

In mole fraction (x)	Parameters			
$In_xGa_{1-x}N$	f_t [GHz]	g_m [mS/mm]	$f_{\max}$ [GHz]	$f_{\max}/f_t$
0.10	6.49	313	17	2.6
0.15	10.89	613	22	2.02
0.20	10.83	663	22	2.03
0.30	10.73	693	22	2.05



(a)



(b)

Fig. 7 – (a) *Gain vs frequency;* (b) *Unilateral power gain vs frequency; RF characteristic observed at the different proportion of x in* $In_xGa_{(1-x)}N$.

3.2 Optimization of gate length

In an HEMT, the practical limitations resulting from the fabrication process, material properties, and device design considerations govern the feasibility of adjusting the gate length. The minimum gate length that can be reliably achieved is constrained by the defined resolutions and tolerances of the lithography techniques and material deposition processes used in fabrication [30]. In addition, extremely short or long gate lengths can affect electron mobility and other

performance characteristics. Device design considerations play a role in determining the practical limits, as shorter gate lengths offer higher performance but can introduce difficulties such as higher leakage currents and parasitic capacitances.

Scaling down the length of the gate in HEMTs also introduces scaling challenges, such as short-channel effects, drain-induced barrier lowering, and gate leakage. These effects can have detrimental effects on device performance, threshold voltage control, and power efficiency. Frequently, advanced process technologies and design techniques are required to address these obstacles. To achieve the desired characteristics of the HEMT, designers must carefully consider the trade-offs between performance, power consumption, and manufacturability while optimizing the gate length [31, 32]. In this section of the paper, we present GaN HEMTs on SiC with various gate lengths for maximum efficiency. AlGaN/InGaN/GaN HEMTs with gate lengths of 0.40μm, 0.50μm, 0.90μm, and 1.0 μm were simulated with a gate width of 100 μm and a drain-source spacing of 4.45 μm. The In proportion was taken as 0.15 as we saw in the previous section it gave the highest f_t value so $In_{.15}Ga_{.85}N$ was taken. Fig. 8 shows drain current vs gate voltage curve and Transconductance vs gate voltage curve for different gate lengths respectively.

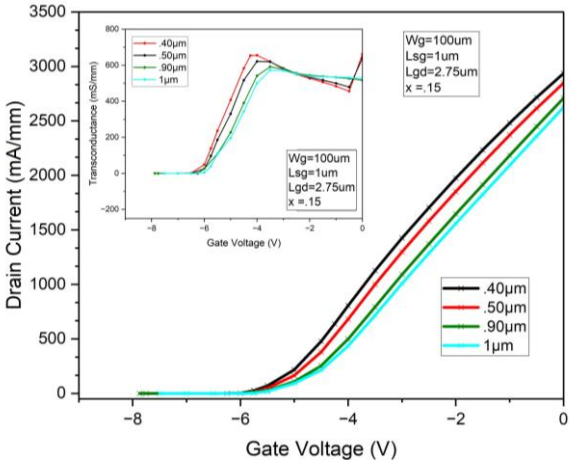
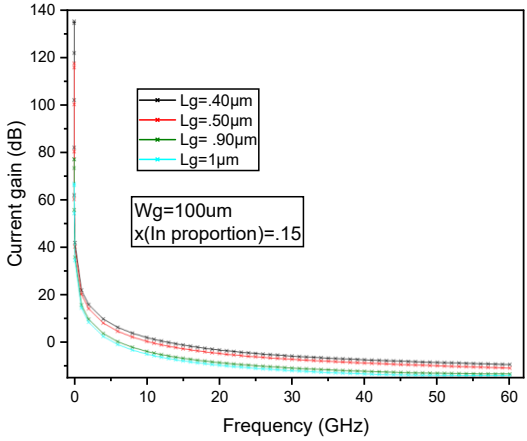


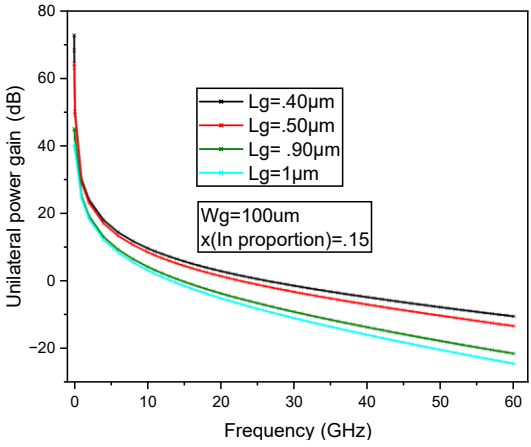
Fig. 8 – *DC transfer characteristics for different gate lengths [Drain current vs Gate voltage curve at V_d=15V].*

The I_d-V_g curve depicts that on increasing the gate length from 0.40μm to 1.0μm the V_t (threshold voltage) shifts towards the right. A lower threshold voltage is generally better for transistors, as it allows them to be switched on with a lower gate voltage. This can lead to improved performance and efficiency. However, there are some trade-offs to consider. Later we plotted the unilateral

power gain U and the short circuit current gain (H_{21}) to study the effect of the gate length change on RF characteristics. As depicted in Figs. 9a and b, the cutoff frequency f_t and the maximum oscillation frequency $f_{\max}$ are determined by plotting these two parameters versus frequency.



(a)



(b)

Fig. 9 – (a) *Gain vs frequency;* (b) *Unilateral power gain vs frequency; Different RF characteristics observed by changing the gate length.*

As shown in **Table 3**, it was reported that the f_t and $f_{\max}$ values are decreased in acceptable limits and so is the g_m value. The best performance $f_t = 13\text{GHz}$ and $f_{\max} = 26\text{GHz}$ was achieved at 0.40 μm gate length.

Table 3
Comparison of f_t and f_{max} for different gate lengths.

L_g [μm]	L_{sg} [μm]	L_{gd} [μm]	f_t [GHz]	f_{max} [GHz]	f_{max}/f_t	g_m [mS/mm]
0.40	1.15	2.9	13	26	2.0	653
0.50	1.10	2.85	10.89	22	2.02	621
0.90	0.9	2.65	6.467	14	2.16	591
1	0.85	2.6	5.90	13	2.20	572

3.3 Optimizing by changing InGaN layer thickness

Several factors limit the maximum thickness of the InGaN layer in GaN/AlGaN HEMT structures. The strain relaxation and lattice mismatch between InGaN and GaN/AlGaN layers, which can lead to the formation of dislocations and a decrease in device performance, are essential factors to consider—maintaining low dislocation density and minimizing strain-related issues by keeping the InGaN layer thickness within an acceptable range [33, 34]. In addition, the maximum layer thickness is determined by the desired material properties and device performance requirements, as thicker InGaN layers may have a lower optical emission efficiency. In addition to the growth technique and crystal quality, the achievable thickness is also determined by the growth technique and crystal quality. Determining the maximum InGaN layer thickness in GaN/AlGaN HEMTs requires experimental optimization and device structure characterization. Also, the critical relaxation thickness of an InGaN channel grown on a GaN buffer can be calculated using the model proposed by Fischer [35]. From the work done by Yachao Zhang et al. [36] given by the (9), (10) and (11), we can have the acceptable range of InGaN thickness.

$$d \approx b/2\varepsilon\,, \tag{9}$$

$$\varepsilon = \frac{a_{\mathrm{InGaN}} - a_{\mathrm{GaN}}}{a_{\mathrm{InGaN}}}\,, \tag{10}$$

$$a_{\mathrm{InGaN}} = a_{\mathrm{InN}}x + a_{\mathrm{GaN}}(1-x)\,. \tag{11}$$

Fig. 10 shows drain current vs gate voltage curve and Transconductance vs gate voltage curve for different channel layer thicknesses.

Table 4 shows the tabulated results of the simulation when the different InGaN thicknesses varied. It is observed that the best transconductance, cutoff frequency, and maximum frequency of oscillation is observed at 2nm.

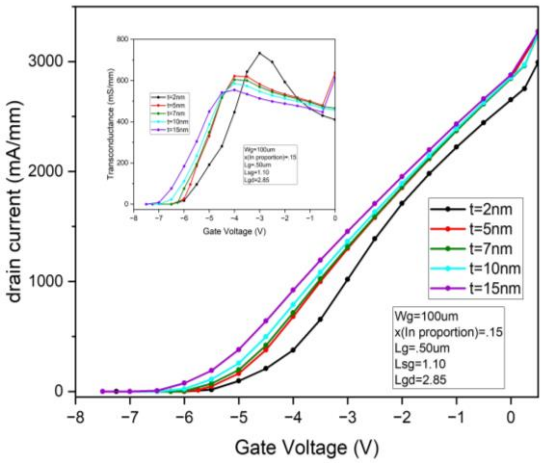


Fig. 10 – *DC characteristics for different thicknesses of* InGaN *layer [Vd* = 15V*].*

Table 4

Comparison of different parameters for different InGaN *thicknesses.*

In_xGaN Layer Thickness [nm]	g_m [mS/mm]	f_t [GHz]	f_{max} [GHz]	f_{max}/f_t
2	732	11.91	23	1.93
5	621	10.89	23	2.11
7	604	10.65	22	2.06
10	585	10.47	22	2.10
15	554	10.32	21	2.03

3.4 Optimization of gate to source length and gate to drain length

Optimizing the distance between source and drain in HEMTs offers several significant advantages. Decreasing the length between the source and drain reduces parasitic capacitances and resistances, resulting in an improved high-frequency performance with a higher f_t and f_{max}. This makes HEMTs suitable for signal processing and communication applications requiring high speeds. In addition, optimizing these lengths improves the device's transconductance (g_m), enhancing signal amplification [37] and overall performance. Additionally, a shorter distance between the source and drain reduces power dissipation, enhances energy efficiency, and enhances thermal management [38]. High-speed digital circuits and wireless communication systems benefit from the increased switching speeds made possible by optimizing these lengths.

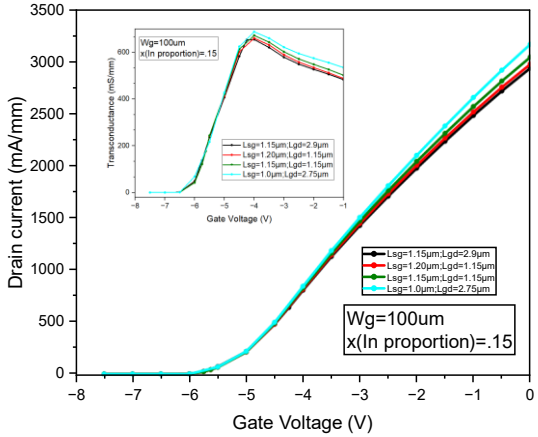


Fig. 11 – *DC transfer characteristics for different gate to source length and gate to drain length [V_d = 15V].*

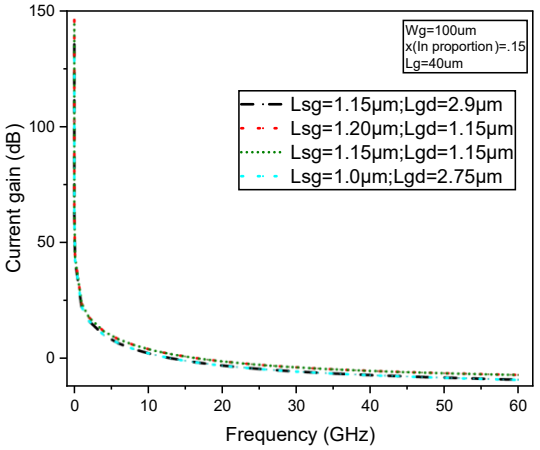


Fig. 12 – *Gain vs frequency.*

Extensive simulations have been performed to find the optimal combination of L_{gs} and L_{gd} dimensions by keeping the gate length constant at 0.40 µm based on previous findings that demonstrated superior performance. Optimized values of L_{sg} and L_{gd} have been considered for which the highest values of f_t and f_{max} are obtained. Consequently, the material composition employed was $In_{0.15}Ga_{0.85}N$. The corresponding DC and RF characteristics for various L_{sg} and Lgd of the device are depicted in Fig. 11 and Fig.12 and 13, respectively. RF characteristic observed at different L_{sg} and L_{gd}.

Table 5 shows the tabulated results of the simulation when the L_{sg} and L_{gd} varied. It is observed that the best cutoff frequency and maximum frequency of

oscillation which are 15.36GHz and 37 GHz are observed at the shortest combination of L_{sg} and L_{gd} which is 1.15µm and 1.15µm respectively.

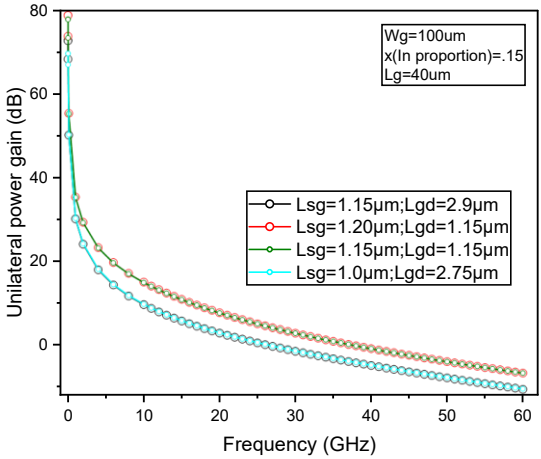


Fig. 13 – *Unilateral power gain vs frequency.*

Table 5

Comparison of different parameters for different L_{sg} and L_{gd}.

L_{sg} [µm]	L_{gd} [µm]	g_m [mS/mm]	f_t [GHz]	f_{max} [GHz]	f_{max}/f_t
1.15	2.9	653	12.90	26	2.01
1.20	1.15	660	15.33	37	2.41
1.15	1.15	672	15.36	37	2.40
1	2.75	687	13.12	26	1.98

3.5 Comparison with the original calibrated device with the optimized device

Table 6 shows a comparison table between the calibrated device and the optimized device DC and RF performance. Fig. 14 represents the schematic view of the optimized device. The comparison table between the calibrated device and the optimized device reveals notable enhancements in both DC and RF performance metrics for the latter.

Table 6

Comparison with the original calibrated device with the optimized device.

Device	g_m [mS/mm]	f_t [GHz]	f_{max} [GHz]	f_{max}/f_t
AlGaN/InGaN/GaN HEMT- calibrated [23]	313	6.49	17	2.6
AlGaN/InGaN/GaN HEMT- optimized	672	15.36	37	2.40

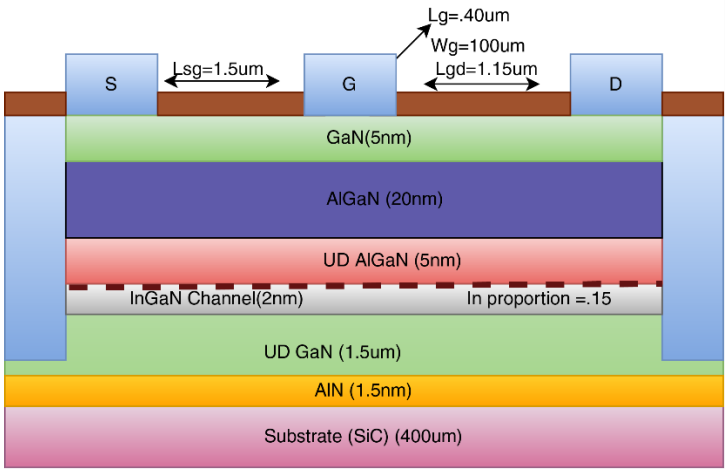


Fig. 14 – *Proposed device structure.*

The optimized device exhibits higher values for transconductance g_m, cutoff frequency f_t, and maximum oscillation frequency f_{max}. This improvement signifies superior electronic characteristics, as higher g_m points to increased signal amplification capability, while elevated f_t and f_{max} indicate enhanced high-frequency response. The significance lies in the optimized device's ability to achieve better signal processing, faster switching speeds, and increased bandwidth, crucial for applications demanding efficient RF performance. Overall, the optimized device surpasses the calibrated one, offering improved capabilities in various electronic applications, particularly those requiring heightened precision, speed, and frequency handling.

4 Conclusion

Using simulation software, this study focuses on the design and characterization of an AlGaN/InGaN/GaN HEMT. The validity of the simulation was established via calibration with experimental data, demonstrating close concordance between the simulated and experimental outcomes. To optimize the device's DC and RF performance, the investigation centred on adjusting four crucial parameters: gate length, In proportion of InGaN, L_{sg} and L_{gd}, and InGaN layer thickness. The optimal values were determined by systematically varying these parameters and conducting exhaustive simulations. The device demonstrated the best performance with a gate length of 0.40μm, an In proportion of 0.15, and L_{sg} and L_{gd} of 1.15 μm and 1.15 μm respectively, and an InGaN layer thickness of 2nm. This study's findings provide valuable insights into the design and optimization of AlGaN/InGaN/GaN HEMTs for various applications. This

research contributes to the development of high-performance devices for applications requiring rapid switching speeds and efficient electron transport by identifying optimized parameters. The study contributes to the advancement in knowledge of AlGaN/InGaN/GaN HEMTs, laying the foundation for future research and development in high-performance semiconductor devices.

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