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*Original scientific paper*

# High-Performance Dynamic Feedback Control-based 8T SRAM using CNTFET Technology

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**Abstract:** Exploration of new materials and device technologies for integrated circuits has become essential due to the exponential growth in demand for high-performance, energy-efficient, and scalable computers. In light of their exceptional electrical and mechanical characteristics, carbon nanotube field-effect transistors (CNTFETs) have emerged as a competitive alternative to traditional Complementary Metal-Oxide-Semiconductor (CMOS) based devices. In this work, a comprehensive overview of recent advancements, challenges, and prospects concerning CNTFET-based Static Random Access Memory (SRAM) cell design. SRAM performance poses significant challenges for VLSI circuits, including power dissipation, operational speed, area efficiency, and leakage current. Technology scaling-induced short-channel effects advocate transitioning from CMOS to CNTFET-based designs. Here, we propose an SRAM design incorporating Dynamic Feedback Control (DFC) features at CMOS 22nm technology nodes. Simulation results conducted using Synopsis HSPICE demonstrate notable enhancements: a 34% reduction in average power consumption, a 95.3% decrease in leakage current, and a 71.6% improvement in delay compared to MOSFET-based SRAM cells. Moreover, energy efficiency for read/write operations improves by 99.6%, and power dissipation is enhanced by 98.5% over MOSFET-based SRAM designs.

**Keywords:** CNTFET, Dynamic Feedback Control, SRAM, Leakage Current, Product innovation, Energy efficiency.

## 1 Introduction

Scaling down VLSI circuits reduces both dynamic and static power [1]. To mitigate power dissipation, switching from unconventional device architectures to innovative circuit topologies is required to expedite the design process. Scaling

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of transistors is advantageous in terms of power consumption but suffers from leakage current, noise sensitivity, soft errors, and performance trade-offs. Traditional SRAMs face challenges with standard activity in the subthreshold range, enabling researchers to investigate Dynamic Feedback Control (DFC) based SRAM cells [2]. These cells offer superior stability and are gaining prominence in traditional research endeavors. Silicon-based transistors have been used in the electronics industry for 60 years due to their dependability, scalability, and manufacturability. However, silicon-based transistors have constraints as technology develops, especially regarding power consumption and nanoscale performance. One of the fundamental drawbacks of silicon-based transistors is that their power consumption increases as transistor sizes decrease. Leakage current is caused by quantum tunneling phenomena and constraints in gate oxide thickness when transistors shrink in size. As a result, power consumption becomes an important concern, especially in portable devices where energy economy is critical, as mentioned in [3].

To address these constraints, researchers have investigated novel materials to be incorporated into transistor architectures. Carbon nanotubes have unusual electrical features, including high carrier mobility and low leakage current, making them potential candidates for next-generation transistors. CNTFETs have various advantages over silicon-based transistors, including lower power consumption, higher performance on smaller scales, and greater tolerance to quantum effects. Furthermore, carbon nanotubes may be produced with precise dimensions and characteristics, enabling customized transistor designs to satisfy specific performance needs mentioned in [4 – 7]. Memory is the most common module found in every electronic device. The fetching of data between the processor and memory is supported by static random-access memory (SRAM). One of the stable architectures of SRAM is based on 6T cells. In this work architecture of the different SRAM cells is investigated using CNTFET, and their performance is explored compared to conventional CMOS-based SRAM. One of the most noticeable advantages is that they have far lower leakage currents, which translates to decreased power consumption, making them ideal for energy-efficient electronics and mobile devices. Furthermore, CNTFETs have outstanding electron mobility, resulting in faster switching speeds and better overall performance of SRAM circuits. Their intrinsic stability and reliability make them less vulnerable to temperature, voltage, and process fluctuations, ensuring data preservation and operational integrity. Furthermore, CNTFETs allow for the manufacturing of smaller SRAM cells, increasing storage capacity without sacrificing performance. Most significantly, they can be integrated into current semiconductor manufacturing processes since they are compatible with complementary metal-oxide-semiconductor (CMOS) techniques. As research continues, CNTFET-based SRAM has the potential to alter memory technology by improving performance, reducing power consumption, and increasing

reliability for future computing systems discussed in [8 – 10]. The novelty of this work lies in Dynamic Feedback Control (DFC) combined with 8T SRAM architecture using CNTFETs. The proposed 8T SRAM architecture shows significant improvement in existing 6T and 7T SRAM cells. No prior work reports such improvement in PDP for CNTFET-based 8T SRAM with DFC under 22 nm technology node.

## 2 About CNTFET

CNTFET utilizes carbon nanotubes as a channel material, offering a promising alternative to traditional CMOS technology. The behavior of CNTFETs can be either ambipolar or unipolar, depending on their structure. In complementary logic design, MOSFET-like CNTFETs are preferred. However, CNTFET technology faces challenges due to process variations, as explained in [11 – 15]. CNTs are highly sensitive to CNT-specific modifications like doping, chirality, diameter, density, and alignment, but less susceptible to changes in the CMOS process. In addition to affecting crucial design constraints like delays, noise margin, leakage current, and stability, ignoring these fluctuations during the design phase might result in severe circuit failures. CNFETs can be fabricated at smaller sizes compared to silicon transistors, enabling better scalability and potentially higher packing density. Carbon nanotubes exhibit high carrier mobility, which means that electrons can move through the channel with less resistance. This property contributes to the high speed. Due to their high carrier mobility, CNFETs can operate at lower power levels than traditional transistors, making them attractive for low-power Carbon nanotubes that possess excellent electrical conductivity and thermal properties contribute to the overall performance. CNFETs can exhibit ambipolar behavior, meaning they can conduct both electrons and holes. This property can be advantageous in certain circuit designs shown in [16 – 18].

CNFETs exhibit fewer short-channel effects compared to silicon transistors, but they tend to have higher defect and failure rates at both the device and circuit levels compared to MOSFETs. CNTFET devices offer advantages over MOSFETs because they have lower quantum capacitance. In MOSFETs, the quantum capacitance keeps increasing, causing higher propagation delay and performance decline. This can improve transistor behavior in smaller devices. Carbon nanotubes also have high thermal conductivity, which helps in effectively dissipating heat from the device. This is important for maintaining device reliability and preventing overheating. Additionally, carbon nanotubes can be synthesized uniformly, resulting in consistent and predictable electrical properties in CNFETs discussed in [20 – 23]. The one-dimensional structure of carbon nanotubes may lead to quantum effects, offering unique possibilities for quantum computing applications. CNFETs can be used in flexible substrates,

allowing for the creation of flexible electronic devices that can bend and flex. Carbon nanotubes have also demonstrated resistance to radiation, which means CNFETs could be useful in tough environments like space or medical imaging devices.

In this work performance analysis of SRAM cells with CMOS and CNTFET. The research utilizes the functionality of the CNTFET model, shown in Fig. 1 and was developed by Stanford University's Nanoelectronics Lab.

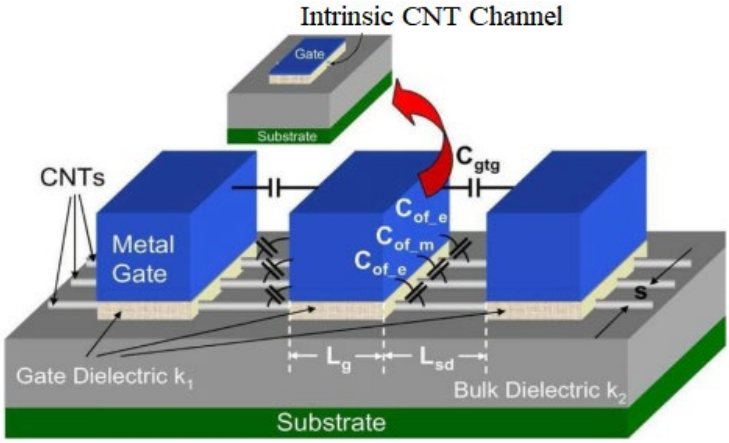


**Fig. 1** – *Schematic View of CNTFET* [19].

The Stanford University CNFET Model is a SPICE-compatible compact representation designed for enhancement-mode, unipolar MOSFETs utilizing semiconducting single-walled carbon nanotubes in their channels. Devices with specific chirality and capable of capturing effects of channel length reduction to 20 nm, the model is grounded in a quasi-ballistic transport, the carrier transport is mostly ballistic (collision-free) but includes non-idealities like photon scattering and parasitics, and encompasses precise characterization of the capacitor network within CNFETs. Addressing practical non-idealities such as carrier scattering due to phonons, parasitic capacitance, and various resistances, this model facilitates circuit-performance comparison, dynamic analysis, and transient response prediction, serving as a valuable tool for CNT circuit exploration and validation [24 – 27]. The diameter of CNTs is a significant parameter that impacts the ON current in CNTFET-based circuits. When the CNT diameter increases, it leads to a reduction in the band gap and a proportional increase in transconductance. As a result, the ON current also increases, as illustrated in Fig. 2.

$$I_{CNTFET} = \frac{Ng_{CNT}(V_{dd} - V_{th})}{1 + g_{CNT} L_s \rho_s}, \tag{1}$$

where $N$ is number of CNT per device, $g_{CNT}$ is transconductance per CNT, $V_{dd}$ is Supply voltage, $V_{th}$ is Threshold voltage of CNTFET, $L_s$ is Source length, $\rho_s$ is Source resistance per unit length of doped CNT.

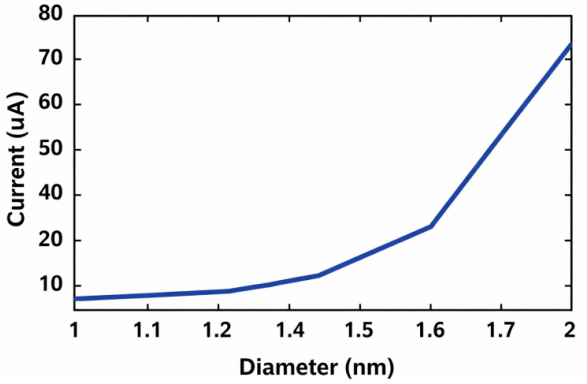


**Fig. 2** – *CNT diameter vs current.*

As the diameter of carbon nanotubes (CNTs) increases, their conductivity improves, but this can negatively impact the power handling capability. Consequently, the power consumption increases, as depicted in Fig. 3.

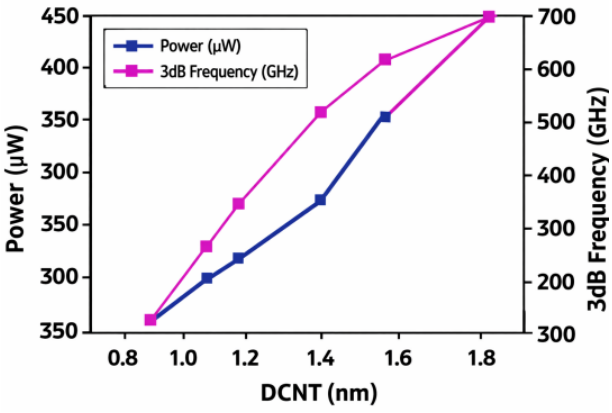


**Fig. 3** – *CNTFET power consumption vs CNT diameter.*

This aspect holds significant importance in designing digital circuits; achieving a high ON/OFF current ratio is crucial for fast device switching and effective control of leakage current [28–30]. The enhancement in the ON current of the device accelerates the switching process, thereby minimizing delays within the circuit, as depicted in Fig. 4.

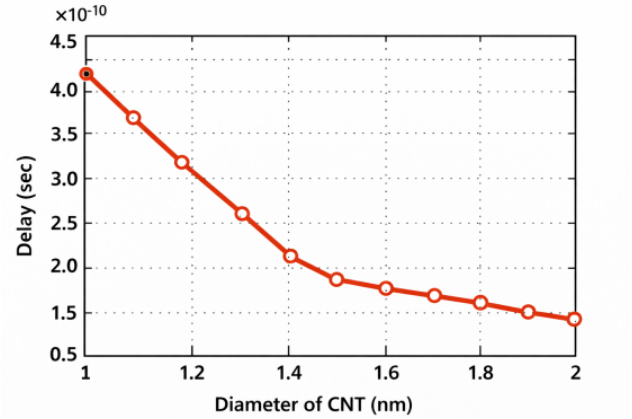


**Fig. 4** – *CNTFET diameter vs delay.*

## 3 Implementation of CNTFET SRAM Cell

Fig. 5 presents an 8T SRAM cell based on conventional CMOS transistors at 22 nm technology. An 8T SRAM cell utilizing CNTFETs with Dynamic Feedback Control (DFC) is an innovative memory cell design that combines the benefits of 8T SRAM architecture with the superior properties of CNTFETs and the advantages of DFC for enhanced stability and energy efficiency. Read and write are majorly operated to access data to and from the cell, respectively.

The first step in writing data into a cell is to activate the word line (WL) that corresponds to the cell of preference. This activates the access transistors and connects the data lines to the storage nodes (bit lines). Depending on the data to be written, the bit lines are driven to the appropriate logic levels (low for logic 0 or high for logic 1). In order to isolate the cell and stop additional modifications, the word line is finally deactivated.

To read data from the cell, the word line of the selected cell is activated, allowing access to the storage nodes. The voltages on the bit lines are sensed to determine the logic levels stored in the cell. If one-bit line voltage is higher than the other, it indicates a logic 1, and vice versa. The sensed data is then amplified and latched for further processing. After the read operation is complete, the word line is deactivated to isolate the cell.

To achieve competitive performance compared to traditional MOSFETs, it is essential to design CNT-based circuits using multiple nanotubes instead of a single nanotube. The selection of the appropriate number of nanotubes becomes a crucial consideration. As depicted in Fig. 5, the PDP in CNTFETs is directly influenced by the CNT counts per device. The oxide thickness, CNT pitch, and supply voltage. The study primarily focuses on CNT diameter and count,

unraveling their effects on ON-current, power consumption, delays, and within the SRAM cell. Through these analyses, the research seeks to refine comprehension of SRAM performance and the implications of CNT-related variables. This presented 8T SRAM cell improves read stability, writing ability, and energy efficiency, demonstrating significant performance benefits over prior CMOS and CNTFET SRAM structures. Unlike conventional 6T/7T designs, this work introduces a stacked inverter layout with bias-controlled feedback paths (FCS1/FCS2). Dynamic Feedback Control (DFC) improves SRAM performance by dynamically adjusting internal feedback paths during read/write operations. By selectively switching off feedback in one inverter during a write, DFC improves write performance by lowering the cell's resistance to state change. DFC improves read stability by preventing internal node instability while reading. Additionally, this dynamic decoupling minimizes needless internal node toggling, which lowers power consumption.

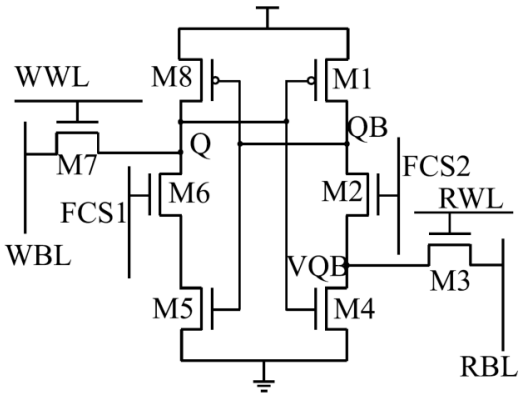


**Fig. 5** – *Single-Ended with Dynamic Feedback Control 8T Subthreshold SRAM Cell* [1].

***1. Improved Read Stability****:* During a read operation, DFC dynamically adjusts the control signals and bias voltages of the read access transistors. It ensures the read operation does not affect the stored bit in the cell and provides more robust read stability.

***2. Enhanced Write Ability:*** DFC applied during write operations optimizes the control signals and bias voltages of the access transistor and improves the write ability of the SRAM cell, allowing for faster and more reliable data storage.

***3. Reduced Power Consumption***: The dynamic adjustments of control signals and bias voltages made by DFC minimize the SRAM cell's power use for both read and write operations. Combined with the inherent benefits of CNTFETs, the 8T SRAM cell with DFC can achieve significant energy savings.

The simulation tool employed in this research is HSPICE, is a widely used Electronic Design Automation (EDA) tool developed by Synopsys.8T CNTFET-based SRAM cell presented in Fig. 6, simulated using the Stanford CNFET model at a CMOS 22 nm technology node.

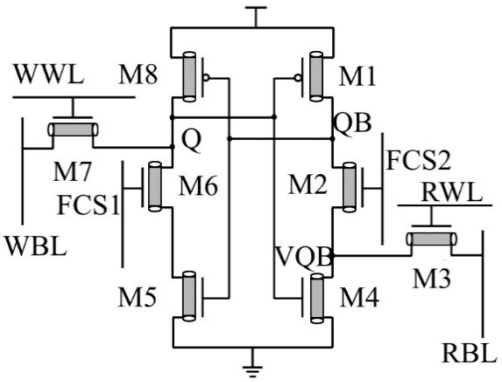


**Fig. 6 –** *SRAM 8T utilizing a CNTFET with Dynamic Feedback Control.*

Compared to the differential6T cell, the proposed 8T cell has fewer cells per bit line and a single-ended read port. Single-ended cells are superior to differential cells in terms of lowering differential switching power during read-write operations. The single cross-coupled inverter pair of the planned 8T consists of three cascaded transistors per inverter. These two stacked cross-coupled inverters, M1–M2–M4 and M8–M6–M5, keep the data in hold mode. A single nMOS transistor M7, which is managed by the write word line (WWL), receives data from a single write bit line (WBL). A separate read bit line (RBL) is used to transfer the data from the cell to the output when the read word line (RWL) is enabled. The FCS1 and FCS2 lines regulate the feedback cutting.

***4. WRITE Operation****:* In 8T cell FCS1 is made low during write 1 operation, turning off M6. Complementary Q (QB) is connected to the ground by M2, which conducts when the RWL is low and the FCS2 is high. Next, if word bit line (WBL) data is applied to 1 and WWL is turned on, current will flow from WBL to Q, increasing Q's voltage through M7, which will write 1 into the cell. Furthermore, the inverter (M1–M2–M4) modifies the state of QB from 1 to 0 when Q changes from 0 to 1. WBL is dragged to the ground, FCS2 is low, and WWL is made high to write a zero at Q. QB is left floating by the low-going FCS2, and it may even get to a tiny negative value before the pull-up current. The cell's operation is dictated by the circumstances of the word lines, bit lines, and control signals, which are depicted in **Table 1**.

**Table 1**
*SRAM cell Operations.*

| | Hold | Read | Write '1' | Write '0' | Row Half Selected | | Column Half Selected | |
|---|---|---|---|---|---|---|---|---|
| | | | | | Write | Read | Write | Red |
| WWL | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| RWL | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| FC1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| FC2 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| WBL | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| RBL | 1 | No Change | 1 | 1 | 1 | 1 | 1 | 1 |

The WRITE BIT in the presented SRAM cell is utilized to write data for logic "0" and "1" values in the SRAM cell. If the data is a logic '1', WBL is set to a low voltage, and WBLB is set to a high voltage. Conversely, if the data is a logic '0', WBL is set to a high voltage, and WBLB is set to a low voltage. The voltage difference between the write bit lines overcomes the feedback loop of the cross-coupled inverters and forces the cell to store the new data value. New data has been successfully stored in the SRAM cell, the write enable (WE) signal is de-asserted, and the write access transistors get turned off, disconnecting the write bitlines from the storage inverters, shown in Fig. 7. The wordline (WL) is deactivated by lowering its voltage level, deselecting the SRAM cell, and completing the write operation. The 8T SRAM cell design enhances the write and read stability of the memory cell by employing distinct write access transistors and read access transistors, which optimizes it for high-performance and low-power applications.

The value of data that will be written to the memory device is determined by the voltage of the WRITE BIT. It is not sufficient to have merely two cascaded inverters in the SRAM cell if the feedback connection is not coupled, as in this case. As in the case of P2, cell data is sent to Q2, and this causes the other inverters (P2 and N2) to produce a Q bar, as in the case of WRITE Each WRITE operation necessitates pre-charging the WRITE BIT to a "high" level before and shortly after the operation. The fact that there is no discharge action at WRITE BIT while writing "0" data means that only a very small amount of writing power is utilized throughout the process.

***5. Simulation Parameters and Assumptions*** The simulations were carried out using Synopsys HSPICE, leveraging the Stanford CNFET compact SPICE model developed by the Nanoelectronics Lab at Stanford University. **Table 2** lists the parameters and conditions that were assumed for the simulation.

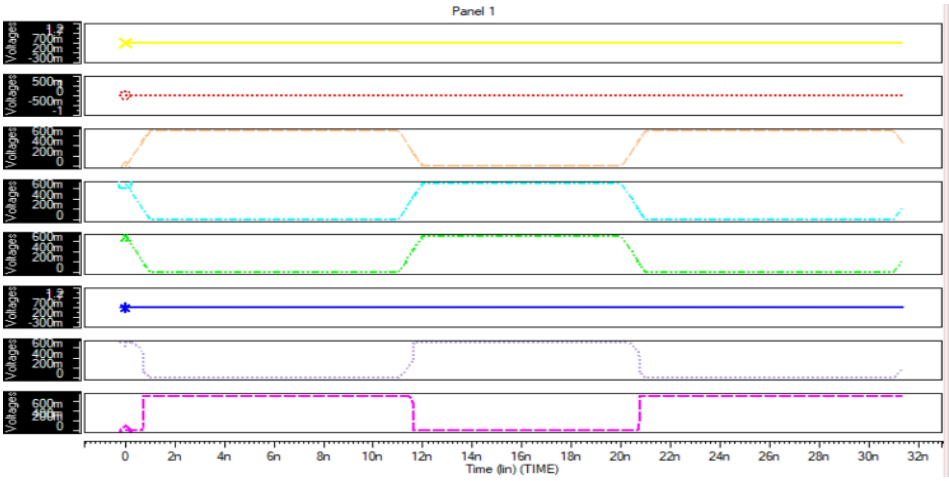


**Fig. 7** – *WRITE Waveform.*

**Table 2**
*CNTFET Simulation Parameters and Assumption* [19].

| Parameter | Value | Description |
|---|---|---|
| Technology Node | 22 nm | Channel length for CNTFET |
| CNT Type | Semiconducting | -- |
| Chirality | (19,0) | CNT diameter of 1.5 nm |
| CNT Diameter | 1.5 nm | Based on Chirality |
| Channel Length | 22 nm | CNT Channel Length |
| Oxide Thickness | 1 nm | Gate Dielectric Thickness |
| Contact Resistance | 10 K kΩ·µm | Source/drain series resistance |
| CNT Pitch | 10 nm | Distance between adjacent CNTs |
| Number of CNT | 3 | Based on drive strength |
| Mobility | Stanford Model default | Ballistic transport assumptions |
| Supply Voltage | 0.8 V | -- |
| Temprature | 25°C | Room temperature |

## 4 Results and Discussion

The performance metrics of the 8T SRAM cell are based on power consumption, delay, and leakage current. A CMOS-based cell consumes 110 nW power and delays 139 ps, SRAM 8T DFC CNTFET exhibits lower values across these parameters, shown in Fig. 8. The average power of the presented circuit is

improved by 34%. The delay associated with an 8T CNTFET-based SRAM cell is primarily influenced by the read, write, and access times of the cell. Due to the high carrier mobility of CNTFETs, the switching speeds are generally faster than those of static CMOS devices, leading to reduced delays in-memory operations. Considering these factors, an 8T CNTFET-based SRAM cell at the 22 nm technology node can potentially exhibit reduced delays compared to conventional CMOS-based SRAM cells, resulting in improved memory access times and overall system performance. Improvement in delay is found at 71.6 % compared to CMOS SRAM cells. These metrics reflect the superior efficiency and performance characteristics of SRAM 8T DFC CNTFET, making it a promising choice for various memory applications where low power consumption and high reliability.

By leveraging the unique properties of CNTFETs, the 8T SRAM cell design can achieve significantly lower power consumption compared to its CMOS counterpart. CNTFETs exhibit reduced leakage currents and improved subthreshold slopes compared to CMOS devices, lower static as well as dynamic power consumption, contributing to more energy-efficient memory operation. The power-delay product (PDP) is an essential metric to assess the energy efficiency and performance of SRAM cells. The PDP comparison in Joules is shown; for the proposed work, it is 99.6 % improved.

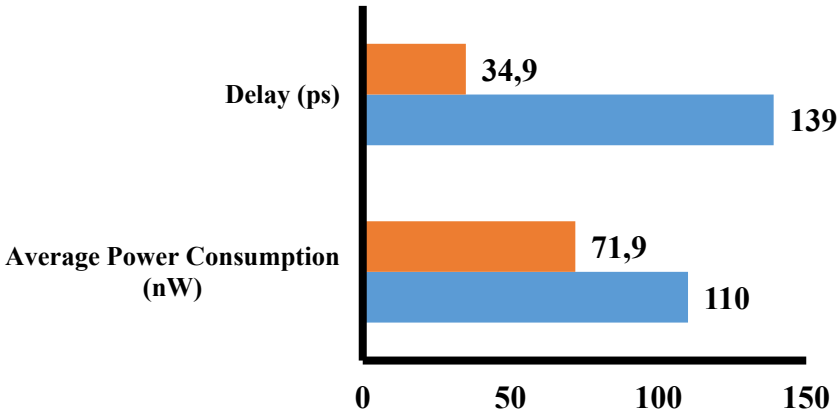


**Fig. 8 –** *Power and Delay Performance of CMOS and CNTFET Cell.*

Leakage current, power consumption, delay time, and power-delay product (PDP) are compared across several SRAMmemory cell types in **Table 3**. The first two rows represent the results obtained from the current study, where two types of SRAM cells, 8T CMOS and 8T CNTFET, are compared. The 8T CMOS cell exhibits a leakage current of 2.54 nA, a power consumption of 110 nW, a delay of

139 ps, and a power-delay product of 15.29×10-21 J. In contrast, the 8T CNTFET cell shows significantly lower leakage current (0.118 nA), power consumption (71.9 nW), delay (34.9 ps), and power-delay product (2.509×10-21 J), indicating improved performance and energy efficiency. The 6T and 7T CNTFET cells from reference [31] demonstrate varying power consumption, delay times, and power-delay products. Similarly, research presented in [32–36] highlights results for CNTFET cells with distinct leakage currents, power consumption levels, delay times, and power-delay products. Overall, the table offers insights into the performance characteristics of various SRAM cell configurations based on CMOS and CNTFET technologies, highlighting the potential of SRAM cells based on CNTFETs to provide faster operation and reduced power consumption.

**Table 3**
*Comparison table of performance metrics.*

| | Cell Type | Leakage Current | Power | Delay | PDP |
|---|---|---|---|---|---|
| This Work | 8T CMOS | 2.54 nA | 110 nW | 139 ps | $15.29 \times 10^{-21}$J |
| This Work | 8T CNTFET | 0.118 nA | 71.9 nW | 34.9 ps | $2.509 \times 10^{-21}$J |
| [31] | 6T CNTFET | -- | 8.75 uW | 5.87 ps | $51.3625 \times 10^{-18}$J |
| [31] | 7T CNTFET | -- | 5.495 uW | 3.604 ps | $19.5 \times 10^{-18}$J |
| [32] | CNTFET | 121.3 nA | 109.2 nW | 3.56 ps | $388.752 \times 10^{-21}$ J |
| [33] | CNTFET | 554 nA | 498.6 nW | 5.89 ps | $2.936 \times 10^{-18}$ J |
| [34] | CNTFET | 307.2 nA | 276.5 nW | 42.27 ps | $11.68 \times 10^{-18}$ J |

To compare CMOS and CNTFET-based SRAM cells in terms of power, delay, and leakage, it's equally important to consider environmental and physical conditions affecting the CNTFET-based circuit performance. A thinner gate oxide improves gate control and transconductance and reduces delay. However, oxide thickness (<1 nm) increases gate leakage and degrades reliability. Simulation results show that Tox from 2 nm to 1 nm improves delay by ~12% but increases leakage by ~18%. Under varying temperatures, 25ºC to 100ºC, CNTFET-based SRAM exhibits ~30% less performance degradation in leakage and delay than CMOS. At temperatures >75°C, leakage current increases exponentially. CNT diameter affects bandgap and thus ON current and power. Larger diameters reduce bandgap, improving ON current but increasing leakage. A smaller pitch increases device density but may lead to inter-CNT coupling and variability. Lower supply reduces power but can affect stability and noise margins in SRAM cells. CNTFETs can operate effectively at lower supply voltages of ~0.4. The presented 8T CNTFET SRAM cell demonstrates improvements in read

stability, power consumption, and PDP, but it also presents limitations. Alignment and chirality control of semiconducting CNTs is a challenge in fabrication. CNTFETs are sensitive to diameter, pitch, and alignment variation, leading to variability in delay and leakage across cells. CNTFETs operate well at low voltage, and significant leakage current flows through access and feedback transistors in idle mode. CNTFET design requires specialized Stanford models

## 5 Conclusion

The presented work demonstrates the 8T SRAM cell based on CMOS and CNTFET transistors. The CNTFET-based SRAM demonstrates lower average power consumption, shorter delay times, reduced power dissipation, lower power-delay product (PDP), and lower leakage current. Compared to CMOS, CNTFET-based cells showed 34% improvement in power, 71.6% improvement in delay, and 95.3% improvement in leakage current value. The utilization of dynamic feedback control (DFC) further enhances the SRAM's stability and dependability, which makes it an acceptable choice for high-performance memory applications where rapid operation and low power consumption meet critical needs. Although CNTFET-based 8T SRAM cells offer advantages in terms of power and delay, their practical implementation is challenged by increased area, fabrication constraints, and variability

## 6 Acknowledgments

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