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Original scientific paper

Co-Optimized E-Mode AlGaN/GaN HEMT with Composite P-GaN Recessed Cap and Etched Doped Buffer for Simultaneous DC and RF Performance Enhancement

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Abstract: This study presents a theoretical analysis of the DC and RF characteristics of enhancement mode (E-mode) AlGaN/GaN High Electron Mobility Transistor (HEMT) utilizing symbiotic integration of advanced techniques e.g. composite gate structure with slightly etched buffer. Enhancement-mode (E-mode) GaN HEMTs often face a fundamental trade-off: achieving high positive threshold voltage (V_{th}) typically degrades RF metrics such as lower cut-off frequency (f_T) and deteriorated transconductance (g_m). To overcome these issues with practical implications, this expedite structure is introduced. The performance analysis is done using TCAD ATHENA to etch, doped, diffusion, and deposition of the architecture as well as TCAD ATLAS to characterize the DC and RF performance. Conventional methods solely focus on individual techniques such as P-GaN caps, recessed gate, buffer etching or doping. This work proposes a synergistically engineered E-mode AlGaN/GaN HEMT which combines these key features: (1) a P-GaN cap, (2) a recessed gate structure, and (3) a slightly etched and carbon-doped AlGaN buffer layer. This combined implementation is only reported in this paper. The device achieves a V_{th} of 2.43 V with higher g_m around 325 mS/mm. This ensures the device remains off at normal secure condition with better gate control characteristics. The lower on-resistance of 139.4 mΩ·mm indicates it can conduct more current for a given gate voltage, reducing power loss when the device is on. This architecture also attains a breakdown voltage (V_{br}) around 1103 V which points out a better threshold performance metrics. Under

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small signal analysis at 1 MHz, key findings have achieved include maximum current of 630 mA/mm, a cut-off frequency of approximately 40 GHz. This simultaneous optimization of DC and RF metrics addresses limitations of prior E-mode designs and makes the device suitable for advanced RF and microwave applications.

Keywords: Enhancement-mode, Etched AlGaN buffer, Sub-threshold swing, Transconductance, Cut-off frequency, Breakdown voltage, On-resistance.

1 Introduction

Gallium Nitride based High Electron Mobility Transistor (GaN HEMT) is a wide bandgap semiconductor device broadly employed in diverse domains like power electronics, radio frequency (RF) communication, high-frequency and high-power applications due to its superior efficiency and ability to function at elevated voltages and temperatures [1 – 4]. Owing to the substantial presence of two-dimensional electron gas (2DEG) induced through polarization at the surface between the barrier and channel layer, GaN HEMTs are mainly depletion-mode (normally-on) device [5, 6]. However, depletion mode GaN HEMTs typically exhibit high gate leakage current and static power dissipation leading to lower overall efficiency of the device [7, 8].

To mitigate these issues regarding depletion mode HEMTs, enhancement-mode (normally-off device) GaN HEMTs are now the focus of interest for the researchers to ensure reliable functionality as well as improvement of the device. E-mode HEMTs have the advantages of less power loss during switching and reduced standby power usage. Their ability to support higher breakdown voltages makes them particularly beneficial in power-sensitive and high-voltage applications [9, 10]. Several methods have been used to achieve a normally-off HEMT (E-mode HEMT), including (a) F-ion implantation technology [11], (b) recessed gate structure [12], (c) P-GaN or P-AlGaN cap technology [13], and (d) polarization cancellation technology [14]. Normally-off device produced by the Fluorine ion implantation terminology causes elevated temperature reliability may be contradictory with practical applications whereas polarization cancellation method attains threshold voltage lower than 1V and may fail to fulfil the modern-day necessities. Larger gate leakage current, gate bias swing are the issues with recessed gate technique [15]. Mohammad Rezaee et *al*. [16], proposed AlGaN/GaN E-mode HEMT with a thin AlGaN barrier layer (thickness of 3nm) and HfLao gate oxide which led to the improvement in threshold voltage to 1.39 V. L. Lino et al. [17] designed an Enhancement mode T-gate HEMT of higher threshold voltage 2.8 V with a breakdown voltage of 633.1 V. Further improvement of breakdown voltage (V_{br} = 1487 V) has been achieved by Hao Wu et al. [18] through step etched GaN buffer structure but the threshold voltage has dropped marginally to 1.1 V. Recently Zhichao Chen et *al.* [9], dedicatedly

researched on the betterment of threshold voltage proposing a normally-off device with an integrated gate structure incorporating a positively cap layer on the etched AlGaN barrier layer where the threshold voltage attains an excellent increased value of 8.6 V with much lower transconductance of 97.5 mS/mm. While Chakrabarty et *al.* [19], focused on transconductance by uplifting the value to 430 mS/mm via designing a fin-shaped tri gate HEMT sacrificing the threshold voltage (V_{th} = 0.5 V) and a lower cut-off frequency of 27 MHz has been found through RF analysis. Therefore, the inherent challenges primarily focus on E-mode devices, where the DC characteristics improve at the expense of RF performance. While the DC characteristics tend to be optimized in E-mode, the RF performance metrics get often degraded. The RF parameters such as f_T, g_m, on-resistance (R_{on}) and parasitic capacitance show better performance in D-mode HEMT compared to E-mode HEMT. So, there is a trade-off between DC and RF characteristics to maintain an optimal balance in E-mode HEMT.

Till now no device has been proposed with desired values of all the parameters at a time. This paper shows a novel structure of composite P-GaN cap and recessed gate with slightly etched AlGaN buffer doped by p-type carbon optimizing the key parameters significantly. In comparison to the conventional HEMT which employs these techniques individually but not in an integrated manner. While each of these elements has been independently explored in prior work, their combined implementation has not been reported. The composite structure of a P-GaN cap with recessed gate is a perfect match for electrostatic control over the channel which reduces drain-induced barrier lowering (DIBL) and maintains a positive threshold voltage (V_{th} > 2 V). In addition, the recessed gate structure minimizes the gate to channel distance as well as lowers parasitic capacitance. Moreover, the P-Gan cap introduces a depletion effect that enhances the threshold voltage to facilitate normally-off operation. The modification of the electric filed distribution, minimization of leakage routes and the improvement of the breakdown voltage is done by buffer etching. The intentional doping of the AlGaN buffer with carbon increases resistivity and traps free carriers to further improve the breakdown performance. These modifications collectively lower the lattice mismatch between AlGaN buffer and GaN channel. This also enhances the DC and RF characteristics of the AlGaN/GaN HEMT. The proposed device shows excellent transconductance (325 mS/mm) with significant breakdown voltage and threshold voltage as P-type doping in the AlGaN buffer increases electron confinement in the 2DEG. The parasitic capacitance is also reduced leading to a better high-frequency response at RF frequencies. From the RF analysis of the device performed at 1 MHz, a very high f_T of 40 GHz has been found. The structure and simulation of the device is illustrated on the device structure as well as in the simulation approach. The findings of the key parameters e.g. cut-off frequency, transconductance, threshold voltage and other DC, RF parameters have broadly discussed on the result and discussion section.

2 Novelty and Contribution

While prior works have investigated P-GaN caps, recessed gates, or etched/doped buffers individually, no report has combined all three. **Table 1** compares literature techniques: our work is the first to co-optimize P-GaN cap, recessed gate, and etched buffer simultaneously. This achieves both $V_{th} > 2$ V and high $f_T \approx 40$ GHz, addressing the DC–RF trade-off unaddressed in previous studies.

Table 1
Comparison of GaN HEMT structures, highlighting their respective advantages and limitations.

Structure	Advantages	Limitations	Ref
Recessed Gate	a) The gate drive circuit for the device is straightforward to implement. b) The ability to adjust the gate dielectric thickness provides a mechanism for optimizing gate breakdown voltage. c) The device's threshold voltage (V_{th}) can be tuned to a maximum value of 1.5 V.	a) Etching introduces surface trap states. b) An inherent trade-off exists between an enhanced threshold voltage and dynamic on-resistance. c) The device requires a complex interface treatment.	[29, 30]
P-GaN gate	a) Gate dielectric is not required. b) The fabrication process is both simple and highly adjustable. c) The device exhibits low leakage current while maintaining good dynamic performance.	a) The threshold voltage is limited to a maximum of 2 V. b) Etching damage outside the gate region leads to a reduction in the 2DEG. c) The device requires protection circuits which deteriorate RF characteristics.	[31]
Step Etched Buffer Layer	a) Alleviates the vertical electric field, which significantly increases the breakdown voltage. b) Improves the crystal quality of the GaN epitaxial layer. c) Reduces surface/interface roughness and threading dislocation density.	a) The process can introduce etching-induced damage. b) May require complex or intricate interface treatment to mitigate the effects of etching. c) Potential for a trade-off between device performance metrics.	[32]

The current state-of-the-art in E-mode GaN HEMT research demonstrates that devices optimized for one performance metric, such as a high threshold voltage or high transconductance, often exhibit degraded performance in others. To date, no single device structure has been reported that concurrently achieves

a high, positive threshold voltage, high transconductance, and an excellent RF response. This work addresses this critical performance gap by proposing a novel, integrated device architecture. The primary contributions are as follows:

1. A Novel Composite Device Structure: This work is the first to report the combined implementation of a P-GaN cap and a recessed gate in accordance with an etched AlGaN buffer within a single device structure. While these elements have been explored independently in prior work, their combined implementation has not been reported in the literature. This composite structure is engineered to provide superior electrostatic control over the channel, which collectively reduces DIBL and significantly enhances the threshold voltage, ensuring reliable normally-off operation.
2. Integrated Buffer Layer Optimization: We further enhance the device performance through the integration of a carbon-doped AlGaN buffer and a slightly etched buffer layer. The carbon doping increases the buffer's resistivity, effectively trapping free carriers and improving the breakdown voltage. The slight buffer etch further modifies the electric field distribution, minimizing leakage paths and collectively lowering the lattice mismatch between the AlGaN buffer and the GaN channel.
3. Simultaneous Optimization of DC and RF Parameters: The unique combination of these structural enhancements leads to the simultaneous optimization of key DC and RF characteristics, overcoming the conventional trade-off. Our simulations demonstrate:
   – An excellent, positive threshold voltage ($V_{th} > 2$ V) for safe, reliable operation.
   – A high transconductance of 325 mS/mm, which surpasses many reported E-mode HEMTs and indicates high gain.
   – A high cut-off frequency (f_T) of 40 GHz, which is a significant improvement in RF performance for this class of devices.

The findings presented in this paper, which are broadly discussed in the results and discussion section, establish a new benchmark for balancing DC and RF performance in E-mode GaN HEMTs and provide a pathway for developing next-generation high-performance devices.

3 Device Architecture

The device architecture is illustrated in Fig. 1. A 300 µm SiC is used as substrate because of its high thermal conductivity and mechanical stability. An AlN nucleation layer of 30 nm is placed above the substrate to ensure high epitaxial growth and reduce lattice mismatch with the succeeding layers. A 2 µm $Al_{0.05}Ga_{0.95}N$ buffer layer is used in the active region which impacts the crystalline

characteristics of GaN channel grown above. 2 µm is chosen to yield a reduced subthreshold leakage. The AlGaN buffer is uniformly doped with carbon at 3×10^{17} cm^{-3} (p-type) to render it semi-insulating and enhance breakdown voltage. A 100 nm GaN channel layer is positioned above this buffer layer which ensures reduced leakage and stable 2DEG confinement[3]. The 15 nm $Al_{0.23}Ga_{0.77}N$ barrier layer is situated above the channel with mole fraction of Al is preserved at 23 %.

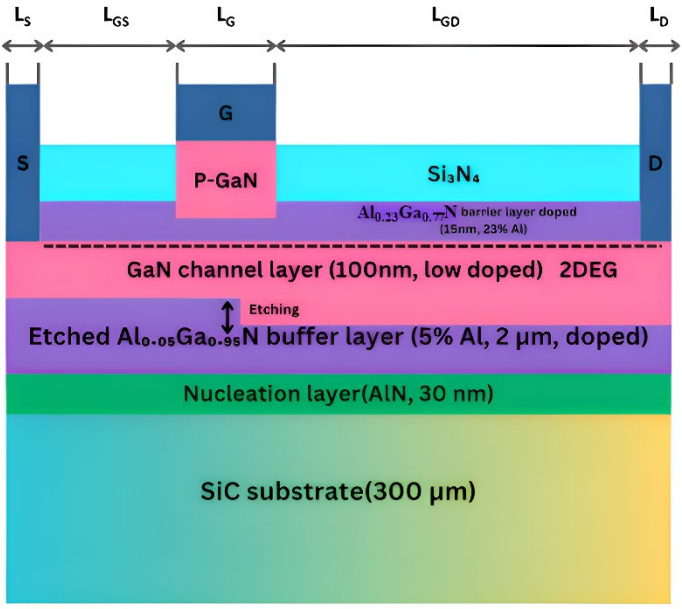


Fig. 1 – *The schematic cross-sectional representation of AlGaN/GaN HEMT including a composite P-GaN cap and recessed gate.*

The mole fraction of Al in buffer is typically lower than the mole fraction in barrier layer. GaN cap layer is positively doped with Mg at 5×10^{17} cm^{-3} concentration is placed at the top of the $Al_{0.23}Ga_{0.77}N$ barrier layer. A small portion of P-GaN cap is recessed down the barrier layer which ensures the enhanced positive gate threshold. A gate length of 0.8 µm and height of 110 nm is positioned around the passivation layer[4]. Si_3N_4 is used as passivation layer to alleviate the surface trap. The values of the device structure dimensions are provided in **Table 2**. Silvaco ATLAS-based TCAD modelling is used for conducting device simulations. The etching process is done by using Silvaco ATHENA TCAD. The Poisson and Schrödinger equations are applied at each node in the final mesh after dividing the structure into smaller segments [19].

[3]A 100 nm GaN channel ensures reduced leakage and stable 2DEG confinement.
[4]A Gate length of 0.8 µm was selected to achieve high-frequency performance (~40 GHz f_T).

These equations provide the fundamental principles necessary for simulating devices in the ATLAS environment.

$$-\frac{\hbar}{2}\frac{1}{dz^2}\frac{1}{m^*(z)}\psi(z)+V(z)\psi(z)=E_i\psi(z), \tag{1}$$

$$\Delta D(z)=-[n(z)-\sigma(z)]. \tag{2}$$

Table 2
Specification of $Al_{0.05}Ga_{0.95}N$/*GaN HEMT with the composite structure and etched buffer.*

Parameter	Specifications
Gate length (L_g)	0.8 μm
Source length (L_s)	1 μm
Drain length (L_d)	1 μm
Device length	8 μm
The thickness of p-GaN overlap (L_{go})	8 μm
P-GaN thickness	118 nm
Source-gate distance (L_{gs})	1 μm
Gate-drain distance (L_{gd})	6 μm
GaN channel layer	100 nm
Al composition in $Al_{0.05}Ga_{0.95}N$ buffer	5%
Al composition in $Al_{0.23}Ga_{0.77}N$ barrier	23%

The device structure is fabricated using ATHENA, where a finely tuned mesh supports sequential deposition, diffusion, and etching to achieve a compact integration of gate, drain, and source regions. Simulations were performed in Simulations were performed in Silvaco ATLAS with a nonuniform mesh refined down to 2 nm in the channel and gate regions (finest grid spacing) and about 5 nm in adjacent areas. A mesh sensitivity analysis confirmed that key results (V_{th} and g_m) changed by < 1% upon further refinement. The overall mesh specification for *x* and *y* axis region is given with mesh width = 1000,

```
x.mesh location=-2 spacing=0.5
x.mesh location=-1 spacing=0.5
x.mesh location=0 spacing=0.1
x.mesh location=0.7 spacing=0.2
x.mesh location=1.4 spacing=0.1
x.mesh location=4 spacing=0.5
x.mesh location=7.4 spacing=0.1
x.mesh location=8.4 spacing=0.1,
```

and,

```
y.mesh location=-0.31 spacing=0.05
y.mesh location=-0.21 spacing=0.05
y.mesh location=-0.155 spacing=0.05
y.mesh location=-0.11 spacing=0.05
y.mesh location=-0.05 spacing=0.05
y.mesh location=0 spacing=0.001
y.mesh location=0.0075 spacing=0.002
y.mesh location=0.007 spacing=0.002
y.mesh location=0.008 spacing=0.002
y.mesh location=0.015 spacing=0.0001
y.mesh location=0.0325 spacing=0.005
y.mesh location=0.05 spacing=0.001
y.mesh location=2.05 spacing=1
```

Here the specifications are assessed in micron (μ) unit. The source is in between –1 and –2 region in *x* axis, gate is in between 0 to 1.4 in *x* axis, and the drain in between 7.4 to 8.4 in *x* axis. Convergence tolerance was 10^{-6}. Source/drain treated as ohmic ($\Phi_M = 4.04$ eV), gate as Schottky on p-GaN. Drift–diffusion model with Fermi-Dirac statistics and Shockley–Read–Hall recombination was used. Mesh sensitivity analysis ensured extracted V_{th} with and g_m varied <1% under further refinement. Baseline results were benchmarked published experimental HEMTs. Following fabrication, DC and RF performance is evaluated via ATLAS, which incorporates mobility models such as GaNSat and Albrct to capture field dependent transport behaviours, while polarization–including piezoelectric effects–is represented through a scalable parameter that modulates net polarization.

Convergence during simulation is ensured by initiating with Gummel's method to establish a stable initial guess and then transitioning to Newton's method for rapid, strongly coupled convergence. This hybrid solver scheme improves stability without undue computational overhead. The workflow routinely applies bias stepping and iterative refinement–utilizing LOG, SOLVE, LOAD, and SAVE statements–to maintain accuracy across analyses. Together, these practices result in a compact, robust model capable of delivering reliable DC and RF insights.

The simulation modelling used Fermi-Dirac statistics as the core principle, while the transport equations have been addressed employing the drift-diffusion model. Moreover, the influence of band gap, confines on carrier recombination is examined by the application of the Shockley-Read-Hall (SRH) model. The output characteristics (I_D, V_{DS}) and transfer curve (I_D, V_{gs}) of AlGaN/GaN HEMT are defined by series of equations which relates to the charge carrier densities and electrostatic potential.

$$\mathrm{div}(\varepsilon \nabla \psi) = -\rho \,. \tag{3}$$

This is called Poisson's equation which relates to the electrostatic potential to the space charge density.

$$\frac{\partial n}{\partial t} = \frac{1}{q}\operatorname{div} \boldsymbol{J_n} + G_n - R_n,$$
$$\frac{\partial p}{\partial t} = -\frac{1}{q}\operatorname{div} \boldsymbol{J_p} + G_p - R_p. \tag{4}$$

This is called carrier continuity equation respectively for electrons and holes. Ohmic contacts, including source and drain, have a work function of 4.04 eV.

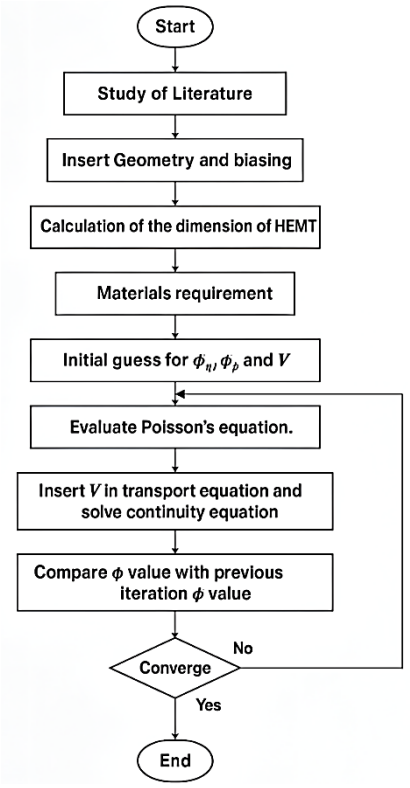


Fig. 2 – *Flowchart of the 2D drift-diffusion (DD) simulation methodology used to analyse the proposed AlGaN/GaN HEMT structure.*

4 Simulation Results of the Proposed Design

The proposed composite device's energy band diagram (Fig. 3) shows a clear band bending at the interface between the AlGaN barrier and GaN channel layers, which makes the 2DEG. This 2DEG serves as a reliable conduction channel as a result of the bending of energy bands in response to an induced electric field.

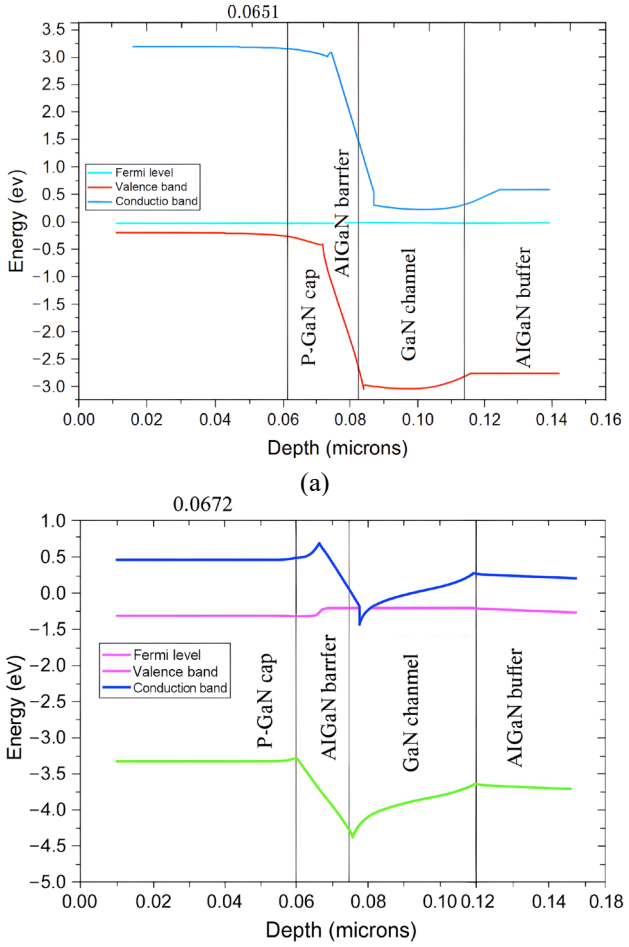


Fig. 3 – *Energy band diagrams of the proposed composite P-GaN cap + recessed-gate HEMT structure in* (a) *off-state and* (b) *on-state. The conduction band (E_C) profile is shown for each bias condition, illustrating the band bending under the gate. In* (a) $V_{gs} = 0$ *V, the P-GaN cap depletes the channel, raising the band and preventing 2DEG formation (device off). In* (b) $V_{gs} > V_{th}$, *the band bends downward, allowing a 2DEG to form at the AlGaN/GaN interface (device on).*

Furthermore, the capacity to enable precise carrier confinement is essential for achieving most effective switching performance. The device's conductivity can be precisely controlled by adjusting the 2DEG density via gate voltage (V_{gs}). This critical component is instrumental in the device's exceptional performance, as evidenced by its transfer characteristics and a variety of operational metrics.

The composite P-GaN cap, the gate recess, and doped buffer layers jointly modify the energy band and carrier transport behaviour of the device. At zero or low gate bias, the P-GaN cap depletes electrons by raising the valence band under the gate, thus increasing the built-in potential and preventing formation of a 2DEG. The gate recess thins the barrier layer beneath the gate, reducing the barrier height for electrons when the gate is biased positively.

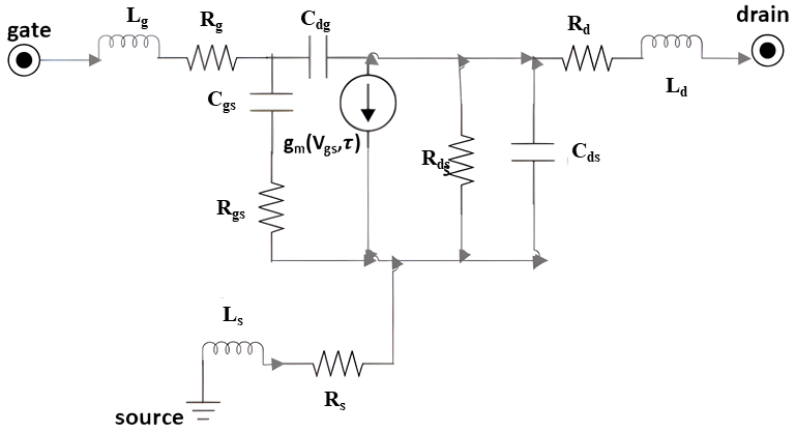


Fig. 4 – *Small-signal equivalent circuit model of the proposed HEMT with the intrinsic transconductance (g_m), gate-source overlap capacitance (C_{gs}), gate-drain capacitance (C_{gd}), drain-source capacitance (C_{ds}), and parasitic resistances (R_g, R_s, R_d), among other elements which represent the device's internal capacitances and resistances that determine its high-frequency behaviour.*

In addition to this capability, the transfer characteristics (Fig. 5) illustrate the device's normally-off operation, as indicated by its positive threshold voltage (2.43 V). The p-GaN cap depletes electrons at the AlGaN/GaN interface by introducing holes, while the recessed gate thins the barrier under the gate, reducing gate-to-channel distance. Together, these effects shift the threshold voltage positively, enabling reliable normally-off operation. As the gate bias increases past threshold, the conduction band under the gate drops, enabling electrons to accumulate at the AlGaN/GaN interface. The carrier transport in this regime is governed by the 2DEG density, mobility, and scattering mechanisms. Interface roughness, remote charge scattering from dopants (e.g., carbon or other acceptors in doped buffer), and polarization induced charges all play roles in limiting mobility and transconductance.

This differentiates the proposed device from traditional HEMTs, which frequently demonstrate normally-on behaviour, rendering them less suitable for power applications. The composite design results in an advantageous threshold voltage, improves carrier confinement, and reduces leakage.

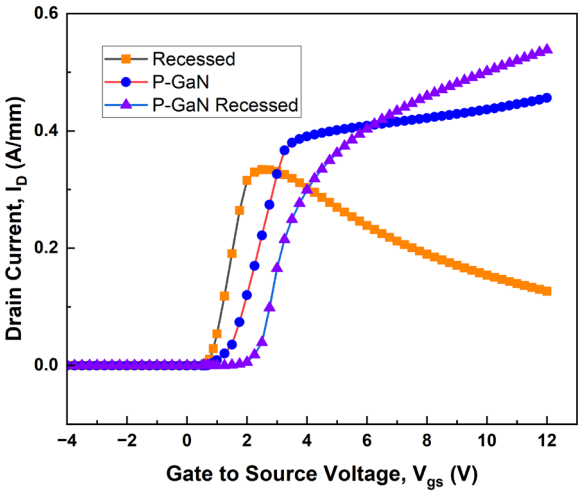


Fig. 5 – *Comparison of transfer (I_D vs V_{gs}) characteristic curves for different device structures under the same bias conditions.*

The output characteristics of the enhancement-mode device is illustrated in Fig. 6. It shows the drain current (I_D) vs drain voltage (V_{ds}) for several fixed gate voltages. Each curve exhibits a linear region at lower drain voltages where the I_D is linearly proportional with $V_{DS,}$ signifies ohmic behaviour. Despite of increasing the drain voltage at the saturation region, the I_D remains saturated and slightly changes with the increase of V_{ds}.

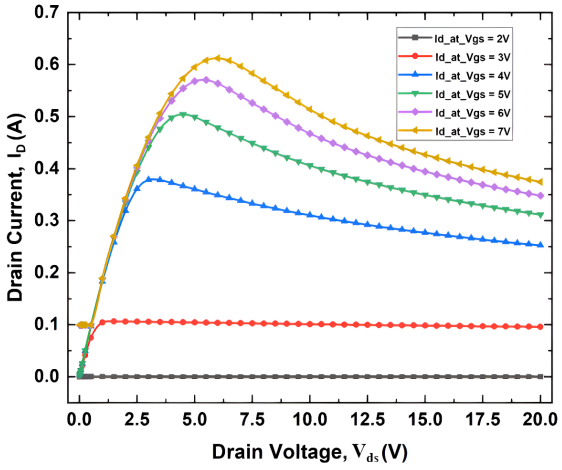


Fig. 6 – *Simulated output characteristics (I_D vs. V_{ds}) of the composite P-GaN cap / recessed-gate / etched-doped buffer AlGaN/GaN HEMT structure for several gate voltages.*

The saturation current is higher for higher gate voltages (V_{gs}). Remarkably, the device shows normally-off operation, as evidenced by the relatively low current level at $V_{gs} = 2$ V and a significant current elevation at higher gate voltages. The output characteristics indicate robust electrostatic control and reliable operation of the composite AlGaN/GaN device in its E-mode design. Field spreading by the doped buffer stabilizes saturation; strong gate control reduces short-channel effects. Under high drain bias, the doped buffer region with acceptor states traps free electrons, which reshape the vertical field distribution. This reduces peak electric fields near critical junctions (e.g., drain-buffer, gate edge), improving breakdown voltage and suppressing leakage. However, these traps may also introduce dynamic effects: charges may not immediately release when conditions change, causing hysteresis, threshold voltage shifts or current collapse under transient or switching conditions.

The device reaches a maximum I_D of 630 mA (Fig. 6), paired with aremarkably low sub threshold swing (SS) of 40.57 mV/decade (Fig. 7). The SS value for P-GaN structure is 94.49 mV/decade whereas in recessed gate structure the value is 86.49 mV/decade. Steep SS arises from strong gate-channel coupling and suppressed leakage paths by carbon doping. This defines the composite device is an exceptional choice for applications that necessitate both high-speed operation and minimal power consumption, as the integration of precise switching characteristics and enhanced drive current ensures energy-efficient performance.

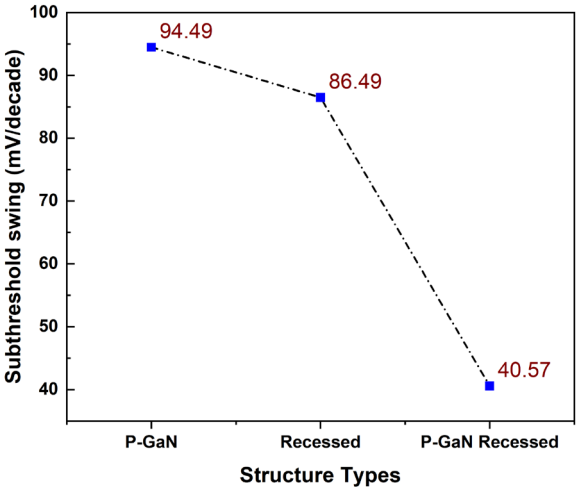


Fig. 7 – *Calculated values of subthreshold voltage swing for different gate structures.*

The graph in Fig. 8 shows that the P-GaN recessed structure achieves the highest $I_{D(ON)}$ and lowest $I_{D(OFF)}$, highlighting its superior on-state current and minimal leakage for improved efficiency and reliability. $I_{D(ON)}$ for p-GaN

recessed gate is 0.5145 A/mm and $I_{D(OFF)}$ is 8.85×10^{-14} A/mm which indicates the lowest leakage current ensures higher safety for circuit operation unlike particularly p-GaN, recessed structures where the leakage is 1.64×10^{-12} A and 2.51×10^{-12} A which is greater than composite structure's leakage.

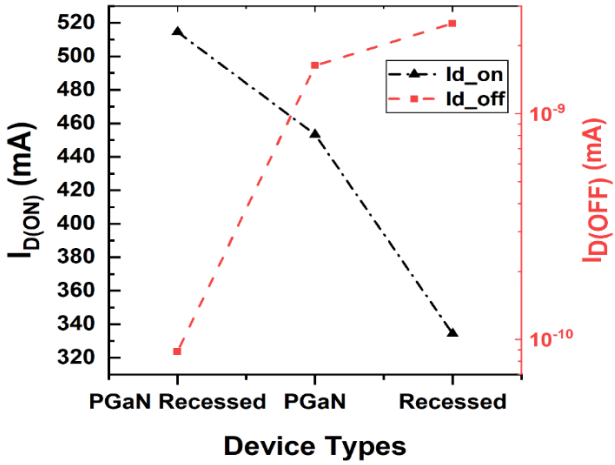


Fig. 8 – *Comparison of **on-current** ($I_{D(ON)}$) vs **off-current** ($I_{D(OFF)}$) for various device structures of the AlGaN/GaN HEMT under identical biasing conditions.*

Moreover, the device's breakdown characteristics are depicted in Fig. 9. The introduction of an etched AlGaN buffer, along with the P-type doping of the buffer, leads to a notable increase in the V_{br} (Breakdown Voltage), rising from 765 V in the non-etched structure to 1103 V in the etched buffer. Etching the buffer reduces the vertical leakage current and buffer induce charge accumulation which enhances the V_{br}. In addition, AlGaN buffer is doped with P-type carbon atoms alleviates the V_{br} due to charge depletion, field spreading and reduced impact ionization.

Furthermore, doping contributes to the passivation of surface defects, which reduces scattering and improves the uniformity of the electric filed. This high V_{br} indicates the device undergoes avalanche breakdown (impact ionization in the buffer) rather than punch-through. The combination of a thick, carbon-doped buffer and reduced leakage paths prevents premature punch-through, so breakdown occurs when the critical field triggers avalanche in the buffer. These characteristics bolster suitability for high-power applications as a result of these combined effects.

The ability of the device to accurately control channel conductivity is additionally, illustrated by its transconductance performance (Fig. 10). The device's design enables a strong electrostatic control, as evidenced by the impressive value of 325 mS/mm near V_{th}. The recessed gate lowers parasitic capacitances (C_{gs}, C_{gd}) and strengthens gate-channel control, enabling better

modulation of the 2DEG and yielding a high transconductance. At the same time, the composite structure maintains an efficient conduction path despite the increased V_{th}, resulting in a relatively low R_{on} of 139 mΩ·mm.

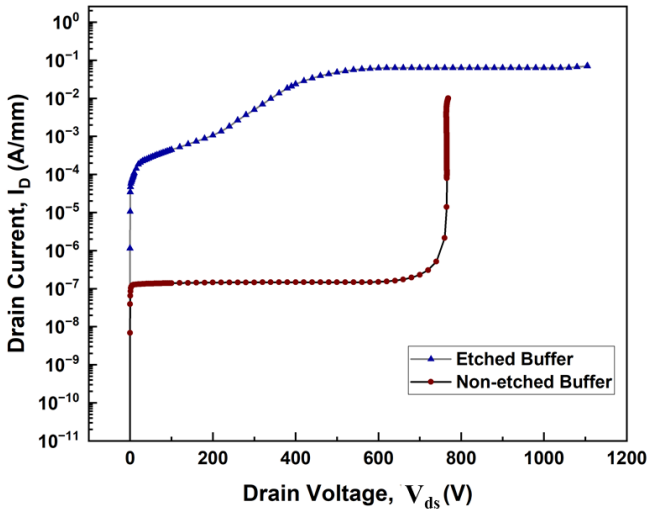


Fig. 9 – *Simulated breakdown voltage curve comparison of etched and non-etched AlGaN buffer layer.*

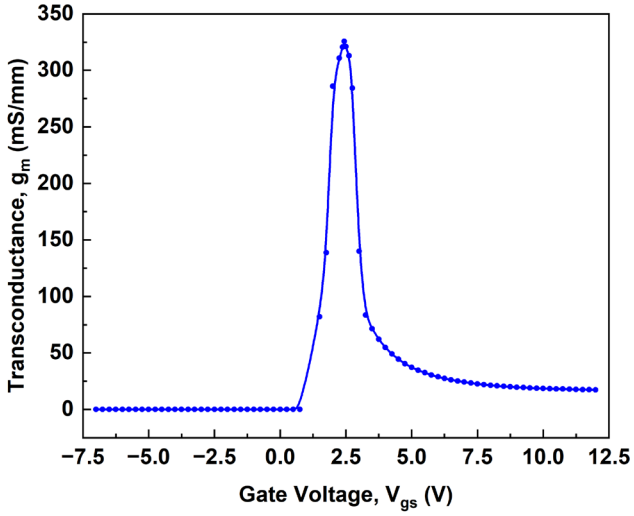


Fig. 10 – *Simulated transconductance curve for composite P-GaN cap and recessed gate technique.*

The ability of the device to accurately control channel conductivity is additionally, illustrated by its transconductance performance (Fig. 10). The

device's design enables a strong electrostatic control, as evidenced by the impressive value of 325 mS/mm near V_{th}. The recessed gate lowers parasitic capacitances (C_{gs}, C_{gd}) and strengthens gate-channel control, enabling better modulation of the 2DEG and yielding a high transconductance. At the same time, the composite structure maintains an efficient conduction path despite the increased V_{th}, resulting in a relatively low R_{on} of 139 mΩ·mm.

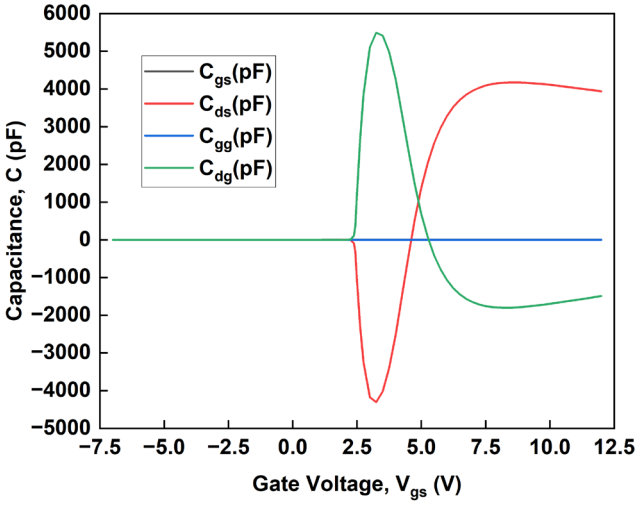


Fig. 11 – *Simulated small signal gate capacitances (C_{gs}, C_{ds}, C_{gg}, C_{dg}) of the proposed structure.*

The capacitance-voltage (C-V) characteristics in Fig. 11 reveal key aspects of the device's high-frequency performance. The stable gate-source capacitance (C_{gs}) indicates strong junction characteristics, while the peak in drain-source capacitance (C_{ds}) at the threshold voltage (V_{th}) signifies the onset of full channel swing. C_{ds} then decreases, showing the transition from depletion to accumulation. Slight irregularities or "noise" observed in the simulated capacitance curves of Fig. 11 originate from numerical convergence limits within the TCAD solver at bias points near threshold. These small oscillations are common in finely meshed electrostatic simulations where abrupt charge redistribution occurs. The averaged trend, however, clearly represents the correct physical behavior — gate capacitances decreasing as the channel transitions from depletion to accumulation. The small oscillations visible in the simulated capacitance curves arise from numerical convergence limits in the TCAD solver near the threshold region, where rapid charge redistribution occurs within the channel. These oscillations are purely computational artifacts caused by discrete bias stepping and fine mesh sensitivity. They do not represent physical capacitance fluctuations. The constant gate-gate capacitance (C_{gg}) implies minimal impact of gate voltage changes, whereas drain-gate capacitance (C_{dg}) initially increases as V_{th} approaches 2.43 V

before swiftly declining, reflecting the pinch-off effect and shorter effective channel length. The capacitances (C_{gs}, C_{gd}) vary with gate bias due to changes in band-profile: in off-state the gate cap and barrier are depleted (high energy barrier); near threshold as conduction begins, the barrier is partially filled; in strong on-state the 2DEG is fully formed. These variations affect f_T and f_{max}. Parasitic resistances (gate, source/drain access, buffer sheet) also degrade RF performance if not properly minimized. The combination of the composite design of cap and recessed gate enhances gate control and reduces channel resistance, improving stability and efficiency, which are essential for high-speed and energy-efficient applications.

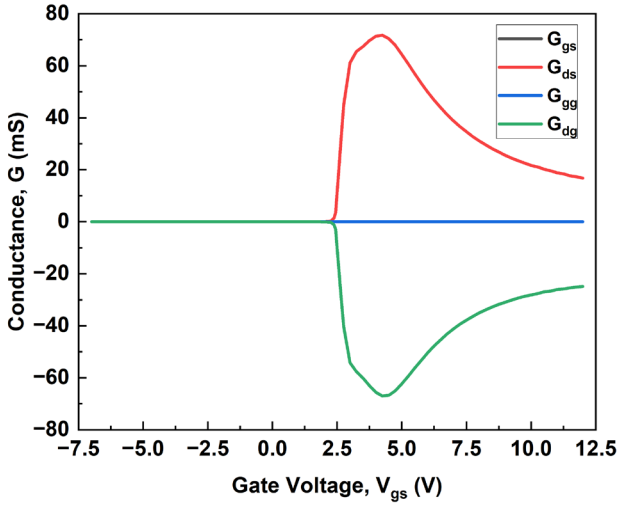
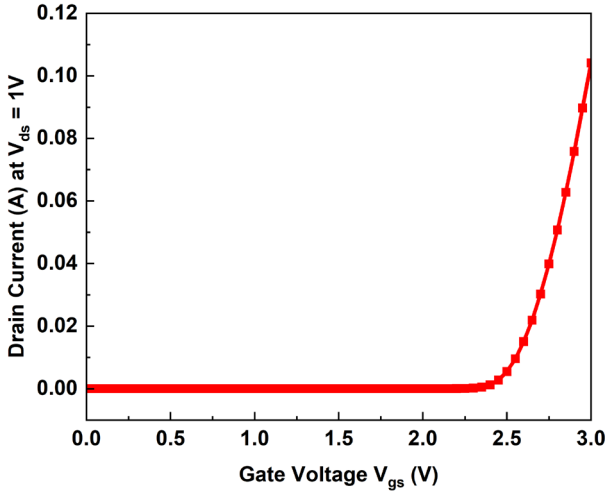


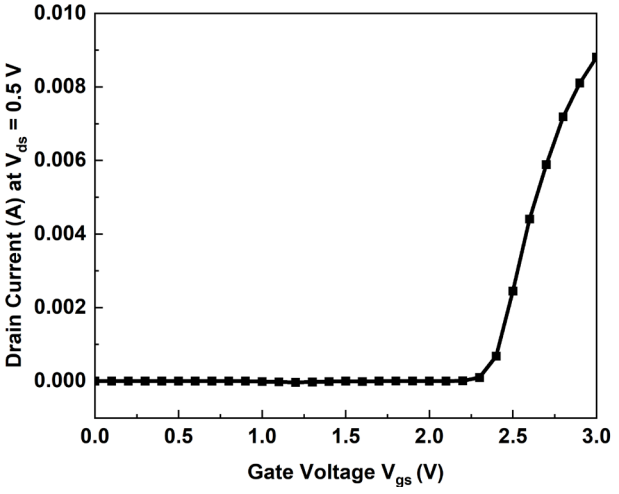
Fig. 12 – *Simulated signal conductances (G_{gs}, G_{ds}, G_{gg}, G_{dg}) of the proposed structure.*

The graph in Fig. 12 (Conductance, G vs V_{gs}) illustrates the transistor's behaviour, showing stable gate-to-source conductance near zero. The drain-to-source conductance (G_{ds}) peaks at 2.43V, signalling saturation. The slight ripple observed in the simulated conductance curves (particularly in G_{ds} and G_{dg}) originates from finite-step bias sweeps and the iterative interpolation between neighbouring bias points in the TCAD numerical solver. These fluctuations reflect solver precision, not any physical instability of the device. The overall conductance behaviour hikes near $V_{gs} \approx 2.4$V and saturation remains accurate and consistent with the expected RF response of the proposed HEMT structure. Notably, the gate-to-drain conductance (G_{dg}) dips at this voltage, indicating reverse coupling before returning to positive, while gate-to-gate conductance (G_{gg}) remains stable. This behaviour indicates effective gate control at moderate V_{gs}, optimizing RF performance and validating the appropriateness for microwave applications.

The exceptional performance is clearly demonstrated by the device's electrostatic integrity, highlighted by its low DIBL (Drain Induced Barrier Lowering) value of 9.5 mV/V. With a 1 V increase in drain voltage, Fig. 13a and Fig. 13b illustrate that the threshold voltage undergoes a mere 4 mV shift as V_{th} from 2.43 V (V_{th1}) to 2.39 V (V_{th2}), indicating exceptional electrostatic channel control. Achieving consistent performance at elevated drain voltages, particularly in high-power scenarios, necessitates the capacity to endure short-channel effects.



(a)



(b)

Fig. 13 *–Transfer characteristics (I_D vs V_{gs}) for a simulated enhancement-mode AlGaN/GaN HEMT with a P-GaN cap and recessed gate, at drain-source voltages (V_{ds}) of* (a) 0.5 V *and* (b) 1 V.

In comparison to conventional HEMTs, which frequently exhibit increased susceptibility to short-channel degradation, the low DIBL performance suggests a significant improvement.

$$DIBL = \frac{V_{th1} - V_{th2}}{1 - 0.5}. \tag{5}$$

Here, V_{th1} is Higher threshold voltage and V_{th2} is Lower threshold voltage.

The device exhibits remarkably strong performance metrics at elevated frequencies. Fig. 14 shows that the cut-off frequency (f_T) of 40 GHz and the maximum oscillation frequency (f_{max}) of 110 GHz significantly exceed the values typically seen in conventional HEMTs. By lowering parasitic capacitances through the recessed structure and enhancing g_m, the device achieves this high cut-off frequency and maximum oscillation frequency. This synergy improves the gain-bandwidth product beyond that of conventional E-mode devices. The capacity to function effectively at these elevated frequencies establishes the device as a strong contender for cutting-edge RF and wireless communication systems.

$$f_T = \frac{g_m}{2\pi C_g}, \; f_{max} = \sqrt{\frac{f_T}{8\pi R_g C_{gd}}}. \tag{6}$$

Excessive buffer etching may create additional traps that degrade reliability, making careful optimization essential. The obtained V_{th} of 2.43 V is moderately higher than most E-mode devices but lower than extreme designs (>8 V), striking a balance that preserves both gm and RF performance.

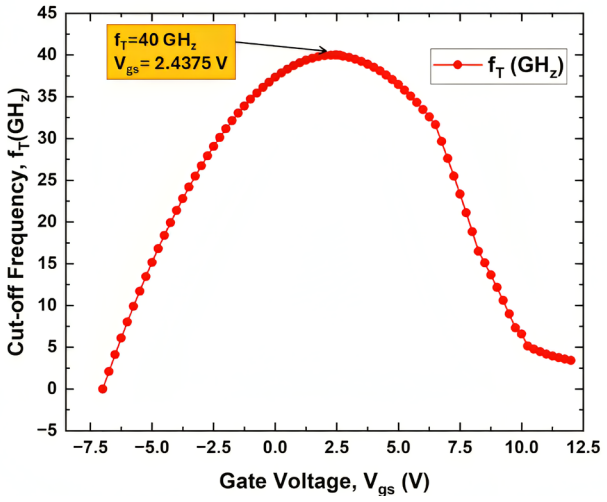


Fig. 14 – *Simulated cut-off frequency (f_T) versus gate-source voltage (V_{gs}), showing the maximum f_T of* 40 GHz *at* V_{gs} = 2.4375 V.

The final table (**Table 3**) provides a comprehensive comparison of device metrics with corresponding prior works. For power switching, the high breakdown voltage and low R_{on} enable efficient and reliable operation at elevated voltages. For RF and microwave use, the moderate V_{th}, strong g_m, and high f_T/f_{max} make the device well-suited for front-end amplifiers and high-frequency circuits. Overall, the design offers a balanced compromise between ultra-high-V_{th} devices, which excel in power safety but lack RF performance, and very low-V_{th}, high-g_m devices, which are fast but less reliable for power switching.

Table 3

Comparison of DC and RF parameters for different structures of GaN HEMT.

Ref	L_g (nm)	g_m (mS/mm)	I_{Dmax} (A/mm)	f_T (GHz)	f_{max} (GHz)	V_{br} (V)	V_{th} (V)	SS (mV/decade)	On/Off Ratio	R_{on} (mΩ·mm)	PAE (%)
[1]	800	511	0.95	122	131	825	–	–	–	4260	–
[9]	2000	97.5	0.718	–	–	–	8.6	–	–	–	–
[16]	4000	–	0.304	–	–	–	1.39	–	11.4×10^{14}	680	–
[17]	1000	232	1.5	49.8	107.8	633.1	2.8	–	–	–	–
[18]	1500	–	0.243	–	–	1487	1.1	–	–	2.718	–
[20]	500	430	1.01	27	90	650	0.5	63	10^{12}	400	–
[21]	250	330	0.85	45	–	–	-3.6	–	–	–	–
[22]	300	425	1.40	55	121	–	–	–	–	–	–
[23]	100	293	0.62	38	75	–	-3.3	–	10^5	–	29.8
[24]	200	260	0.954	38	65	220	-4.1	–	–	400	29.4
[25]	600	370	1.13	26	60	–	–	–	–	–	85.2
[26]	200	245	1.07	55	–	189	-5	–	10^8	–	–
[27]	800	370	0.747	–	–	–	0.3	–	10^4	2.697	–
[28]	2000	–	–	–	–	–	1.224	–	–		–
[33]	4000	_	_	_	_	1192	3.2	_	_	0.0113	–
[34]	450	200	1.000	20	40.8	206	1.1	_	_	1.8	70
[35]	50	541	2.710	391	_	_	_	_	_	_	–
[36]	55	710	5.9	290	364	73	-3	_	_	_	–
This Work	800	325	0.630	40	110	1103	2.4	40.57	5.2×10^{12}	139.4	≈50

Taken together, the composite structure leverages: (1) band-engineering to shift threshold in a desired direction; (2) modulation of barrier thickness and doping to maintain high 2DEG density for large on-current; (3) trapping and buffer design to suppress leakage and increase breakdown, at cost of some dynamic/temporal response. The improvements in on-current, on/off ratio, breakdown voltage, cut-off frequency and transconductance emerge from this balanced optimization of energy band profiles, carrier density, scattering and trap effects. So, the proposed HEMT is an exceptional choice for advanced applications due to its superior breakdown voltage, low on-resistance, and improved high-frequency performance, as demonstrated in the **Table 3**.

5 DC–RF Trade-Offs and Device Limitations

The composite P-GaN / recessed-gate / doped buffer structure introduced in this work offers multiple simultaneous improvements in DC and RF performance. However, these improvements arise through trade-offs and also expose certain limitations which must be considered for realistic device implementation. Below are the key mechanisms, trade-offs, and practical limits:

Physical Mechanisms Enabling Improvements

- Channel depletion and threshold-voltage control: The P-GaN cap introduces built-in depletion that raises the conduction band edge under the gate, requiring a positive V_{th} to form the 2DEG. The gate recess reduces the AlGaN barrier thickness under the gate, so that less barrier material must be biased to populate the channel. Together, these yield a positive threshold voltage while preserving sufficient 2DEG density when on.
- Buffer doping and field spreading: Slight carbon (or p-type) doping of the buffer increases buffer resistivity and introduces acceptor states that trap mobile electrons under reverse bias or off-state conditions. This spreads the vertical electric field more uniformly during high V_{DS}, reducing peak field intensity at drain/buffer interfaces, which increases breakdown voltage.
- Reduced parasitic capacitances for RF: By employing a thin barrier under the recessed gate, and limiting excess capacitances from the P-GaN cap (e.g. capacitance between cap and channel, gate leakage paths), the parasitic gate-to-drain (C_{gd}) and gate-to-source (C_{gs}) capacitances are contained. Lower gate resistance (from geometry or metal layout) also helps maintain high cutoff frequency (f_T) and maximum oscillation frequency (f_{max}).

Table 4
DC–RF *trade-offs*.

Parameter Improved	Sacrifice / Penalty Introduced
Higher threshold voltage and normally-off operation	Lower 2DEG density at zero bias → reduced on-current and possibly lower transconductance if bias is insufficient.
Increased breakdown voltage	Increased buffer resistance, deeper traps → potential current collapse under high bias or dynamic switching, slower transient response.
Reduced parasitic capacitances	Thinner barriers or recesses might increase sensitivity to interface roughness, non-uniform etch, leakage under high gate bias, or dielectric stress in P-GaN cap region.
Higher f_T/f_{max}	Possible trade with stability, gate and drain leakage, and gate capacitance variation under bias; also, fabrication complexity increases (etch, doping control, cap activation).

Device Limitations and Practical Considerations

– Trap-induced dynamic effects: Deep acceptor states (in carbon-doped buffer or P-GaN cap) may trap carriers in off-or partial-on states. Under pulsed or high-power dynamic operation, this can lead to increased effective R_{on} (current collapse), slower turn-on times, or temporary threshold shifts.

– **Interface quality and uniformity:** Recessed gate regions and P-GaN cap interfaces must be fabricated with high uniformity. Any non-uniformity or defects at barrier/cap interfaces increase scattering, degrade mobility, produce leakage paths, and can worsen subthreshold swing or RF gain.

– **Gate leakage and reliability under high bias:** P-GaN gates (Schottky or metal stack) and thin AlGaN barriers can suffer leakage under high gate bias or temperature. Prolonged bias stress may degrade threshold voltage or lead to premature gate breakdown.

– **Parasitic resistances and geometrical limitations:** Even with optimal gate recess and cap design, source/drain access resistances, gate metal resistance, and buffer sheet resistance contribute parasitics that limit f_{max} especially. Further scaling of gate length may be needed, but these risks exacerbating short channel effects or fabrication demands.

– **Thermal management and self-heating:** High current densities and high voltage operation generate significant heat. Because GaN buffers and caps may have thermal conductivity lower than bulk GaN, device

temperature rise can degrade mobility and widen energy band-tail states, affecting DC on current and RF linearity.

– **Temperature Effects:** In realistic operation, elevated device temperature will degrade several key performance parameters of the proposed HEMT structure. As the junction or channel temperature rises, carrier mobility in the GaN channel typically decreases due to enhanced phonon-scattering and increased lattice vibrations, which results in lower drain current ($I_{D(\max)}$) and reduced transconductance (g_m) [37]. Concurrently, on-resistance (R_{on}) tends to increase and threshold voltage (V_{th}) may undergo a slight negative shift, thereby reducing the breakdown voltage margin (V_{br}) and the RF gain at higher temperature. Even though the simulations presented here assume nominal room-temperature ambient conditions, the actual performance at elevated temperature would likely follow a modest reduction in $I_{D(\max)}$ and g_m and a rise in R_{on}, underscoring the importance of effective thermal management in real-world high-power or high-frequency applications.

6 Conclusion

The DC and RF characteristics of a typically off AlGaN/GaN HEMT with a composite structure is examined. A positive threshold voltage of 2.43 V ensures the enhancement mode with reduced gate leakage and low power dissipation. Transconductance peaks at 325 mS/mm and stabilizes post-threshold, indicating promise for RF applications. High breakdown voltage and 139.42 mΩ·mm R_{on} satisfies the stability for operation in the "on" state. The device also has a subthreshold swing of 40.57 mV/decade and a DIBL value of 9.5 mV/V, indicating strong electrostatic control. With a cut-off frequency of 40 GHz and a maximum oscillation frequency of 110 GHz, this device is suitable for high-speed and high-frequency applications. These results indicate its remarkable potential for low leakage, greater enhancement and future RF applications.

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