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Effects of Gate Bias Stressing in Power VDMOSFETs

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Abstract: The effects of gate bias stressing on threshold voltage and mobility in power VDMOSFETs and underlying changes in gate oxide-trapped charge and interface trap densities are presented and analysed in terms of the mechanisms responsible. In the case of positive bias stressing, electron tunnelling from neutral oxide traps associated with trivalent silicon $\equiv Si_o^{\bullet}$ defects into the oxide conduction band is proposed as the main mechanism responsible for positive oxide-trapped charge buildup, while subsequent hole tunnelling from the charged oxide traps $\equiv Si_o^{+}$ to interface-trap precursors $\equiv Si_s$-H is shown to be the dominant mechanism responsible for the interface trap buildup. In the case of negative bias stressing, hole tunnelling from the silicon valence band to oxygen vacancy defects $\equiv Si_o^{\bullet\bullet}Si_o\equiv$ is shown to be responsible for positive oxide-trapped charge buildup, while subsequent electro-chemical reactions of interfacial precursors $\equiv Si_s$–H with the charged oxide traps $\equiv Si_o^{+\bullet}Si_o\equiv$ and H^+ ions are proposed to be responsible for interface trap buildup.

1 Introduction

Power VDMOSFETs are attractive devices for high-frequency switching power supplies in communication satellites, but an important requirement for these applications is their high radiation tolerance. Namely, over the years of communication satellite mission, even in low-Earth orbits these devices can accumulate the total dose up to 10 krad (SiO_2), while in high orbits this dose can be as high as 1 Mrad (SiO_2) [1].

It is well known that the ionising radiation induced gate oxide-trapped charge and interface traps cause the threshold voltage shift, transconductance reduction, leakage current increase, and breakdown voltage reduction in power VDMOSFETs [2-4]. The negative threshold voltage shift is, undoubtedly, the most serious problem in the commercial devices since it may cause a change of their operation mode from enhancement to depletion, thus leading to a faulty operation of switching power supplies. Even the radiation-hardened devices may fail as a result of reduction in current-drive capability owing to channel carrier mobility degradation and/or positive threshold voltage shift [2].

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With increasing utilization of MOS technology for the realization of power devices and ICs, the interest in ultra-thick gate oxides has steadily grown, and investigations of related reliability issues have recently gained in importance [5-8]. Recent investigations by Picard et al. [5, 6] have revealed the effects of gate bias stressing and ionising radiation on electrical parameters of power VDMOSFETs to be very similar (as earlier observed in CMOS devices [9]), but their analysis of responsible mechanisms has remained in the scope of qualitative description. Actually, their work was aimed at utilizing the gate bias stressing for radiation hardening of VDMOSFETs [5] and developing the device selection method for application in radiation environment [6]. The former idea appeared to be completely inapplicable [10], while the latter one sounds promising; in both cases, detailed analysis of mechanisms responsible for behaviour of device parameters during stressing is required.

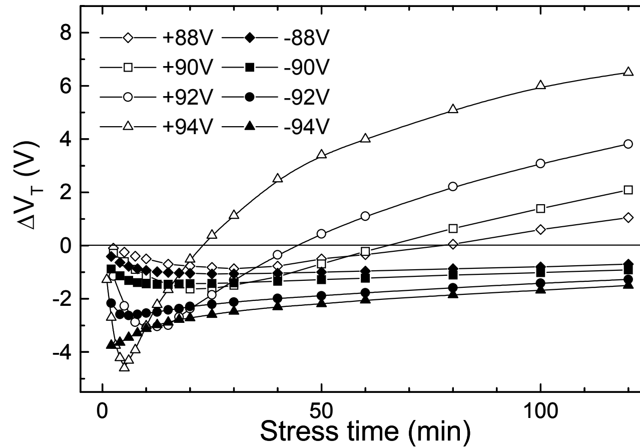
In this paper, the results of our detailed analyses of the effects of gate bias stressing on threshold voltage and mobility in power VDMOSFETs and underlying changes in gate oxide-trapped charge and interface trap densities, are reviewed [10-13]. The data are analysed in terms of the mechanisms responsible for the oxide-trapped charge and interface trap buildup, and the model, which explains in detail the experimental data, is proposed.

2 Results and Discussion

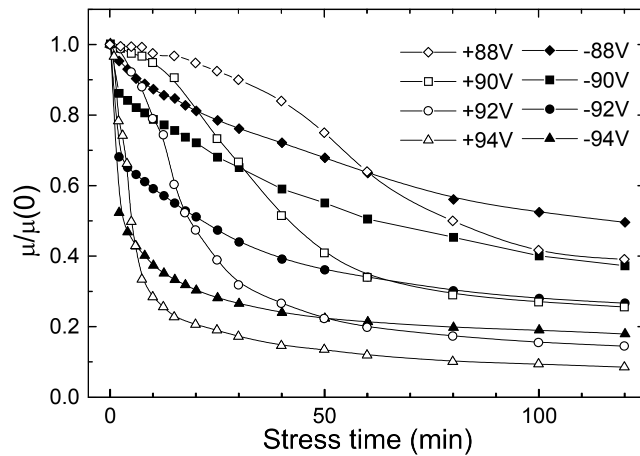
Devices used in this study were commercial n-channel VDMOSFETs built in a standard Si-gate technology (120 nm thick gate oxide grown in dry oxygen) with hexagonal cell geometry. Electrical stressing was performed by applying either positive or negative DC bias (±88, ±90, ±92, and ±94 V) to the gate electrode for 2 hours, with drain and source terminals grounded. To reduce probability of the early oxide breakdown, gate voltage was gradually increased up to a desired value for stressing the device. In order to detect the device response to stressing and analyse underlying mechanisms, an electrical characterization, including the measurements of both subthreshold and above-threshold transfer characteristics in the saturation region, was performed during the device stressing. Additional measurements of the gate current and charge pumping current were also performed during the stressing in order to provide better insight into the mechanisms responsible.

Threshold voltage and channel carrier mobility behaviour in power VDMOSFETs during the electrical stressing is shown in Fig. 1. Values of the threshold voltage and mobility were determined from the measured above-threshold transfer characteristics as the intersections between V_G-axis and extrapolated linear region of $\sqrt{I_D} - V_G$ curves and the slopes of these lines, respectively. As can be seen, both negative and positive gate bias stressing cause similar effects on threshold voltage and mobility in power VDMOSFETs, the effects being more pronounced at higher stress voltages. Namely, there is an initial decrease of threshold voltage followed by its increase (turn-around effect) towards the initial value, while the mobility continuously decreases. In the case of positive bias stressed devices, threshold voltage reaches and even exceeds the initial value (rebound effect). The negative gate bias stressing causes more rapid initial changes of both threshold voltage and mobility, but maximum negative threshold voltage shift (at turn-around

point) is smaller compared to that caused by positive bias stressing. After the turn-around occurs, the rate of these changes becomes considerably lower and final threshold voltage shift and mobility reduction are significantly smaller in devices stressed by negative bias



(a)



(b)

Fig. 1 - *Threshold voltage (a) and mobility (b) behaviour during the electrical stressing of power VDMOSFETs.*

Since the changes of gate oxide-trapped charge and interface trap densities are responsible for the behaviour of threshold voltage and mobility in MOS devices during the electrical stressing [9, 14], it is very important to quantitatively determine these changes in stressed power VDMOSFETs. It should be noted that higher positive stress voltages (+92 and +94 V) resulted in severely distorted subthreshold characteristics (phenomenon already observed in devices exposed to cryogenic temperatures [3] and high radiation

dose levels [15]), and we were not able to apply the commonly used subthreshold midgap technique (SMGT) [16] to devices stressed by these voltages. For that reason we have also used the single-transistor mobility technique (STMT) [9, 14] to determine the changes of oxide-trapped charge and interface trap densities.

The STMT is based on the following model of the stress induced threshold voltage shift and channel carrier mobility reduction [9, 14]:

$$V_T = V_T(0) - \frac{\Delta Q_{ot}}{C_{ox}} + \frac{q\Delta N_{it}}{C_{ox}} \tag{1}$$

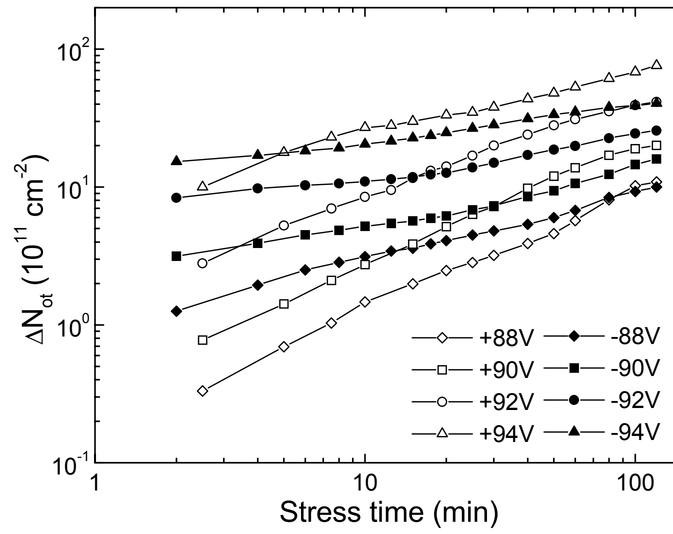
and

$$\mu = \frac{\mu(0)}{1 + \alpha_{ot}\dfrac{\Delta Q_{ot}}{q} + \alpha_{it}\Delta N_{it}}\ , \tag{2}$$

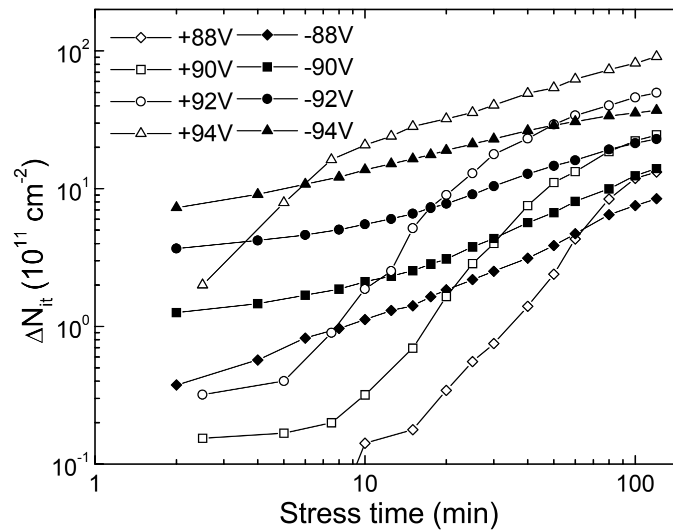
where $V_T(0)$ and $\mu(0)$ are the initial values of the threshold voltage and mobility, respectively, ΔQ_{ot} ($\Delta Q_{ot}=q\Delta N_{ot}$) and ΔN_{it} are stress induced changes of the oxide-trapped charge and interface trap densities, respectively, and α_{ot} and α_{it} are the fitting coefficients in the model for stress induced mobility reduction (α_{ot}=0.0645·10^{-12} cm^2, α_{it}=1.13·10^{-12} cm^2 [17]).

It should be emphasized that, besides the dual transistor mobility technique (DTMT) [18], STMT is the only technique providing the direct correlation between the changes of device parameters and underlying changes in oxide-trapped charge and interface trap densities. Both STMT and DTMT are based on standard measurements of threshold voltage and carrier mobility taken at currents 2-5 orders of magnitude above those required for commonly used SMGT. Therefore, STMT and DTMT do not face the SMGT restrictions associated with non-linearity of subthreshold characteristics at severe stress conditions. Unfortunately, DTMT is not applicable to power VDMOSFETs since it requires both n- and p-channel devices with identically processed gate oxides (preferably on the same chip or wafer), which is never the case in this technology. On the other hand, the only disadvantage of STMT is related to a complicated determination of the fitting coefficients α_{ot} and α_{it}, as well as to a fact that their values are not universal but are dependent on device fabrication process.

The changes in the densities of oxide-trapped charge and interface traps during the stressing, determined by STMT and SMGT, are shown in Figs. 2 and 3, respectively. As can be seen, a significant increase of oxide-trapped charge and interface trap densities is observed for both positive and negative gate bias stressing, the changes being more pronounced at higher stress voltages. It can be noticed in the case of negative gate bias stressing that creation of interface traps begins without any time delay in respect to oxide-trapped charge, i.e. the “threshold” oxide-trapped charge density is not required before the creation of interface traps can start [11, 13]. Moreover, there is more considerable initial buildup of oxide trapped charge and interface traps, but their densities increase at lower rate than in the case of positive gate bias stressing. Consequently, the final changes of both oxide-trapped charge and interface trap densities are lower compared to those caused by positive bias stressing, which is in line with observed threshold voltage and mobility behaviour.

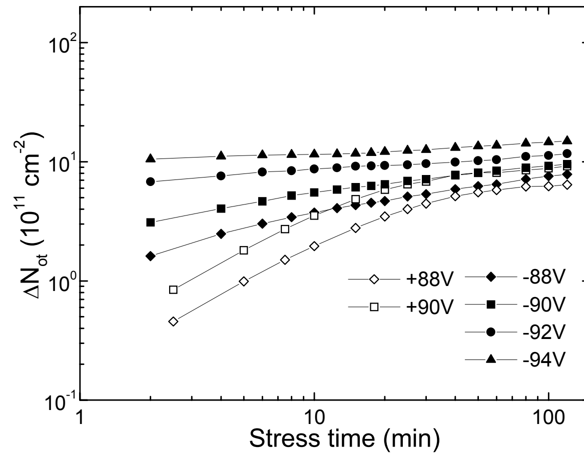


(a)

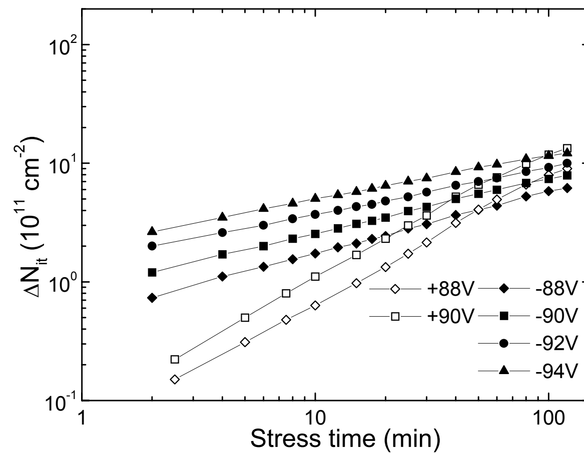


(b)

Fig. 2 - *Changes of gate oxide-trapped charge (a) and interface trap (b) densities during the electrical stressing of power VDMOSFETs determined by STMT.*



(a)



(b)

Fig. 3 - *Changes of gate oxide-trapped charge (a) and interface trap (b) densities during the electrical stressing of power VDMOSFETs determined by SMGT.*

It has been shown that low frequency measurements employed in the above techniques (SMGT and STMT) lead to overestimated densities of "true" interface traps [19] since at low frequencies the border traps can mimic the electrical response of interface traps [20]. That was why for determination of interface trap densities we have additionally used the charge pumping technique (CPT) [21, 22] based on measurements performed at 100 kHz. The CPT has been shown to enable accurate, highly sensitive and direct measurements of interface trap density in different MOSFETs, independently on oxide-trapped charge density. Note that, when applied to power VDMOSFETs, CPT

provides the information on interface above the n$^-$-epitaxial layer, but not directly on interface above the channel.

The CPT results, shown in Fig. 4, revealed very similar behaviour of ΔN_{it} to that obtained by STMT and SMGT (Figs. 2 b and 3 b, respectively), but the values of ΔN_{it} are significantly lower in the case of CPT. The qualitative agreement in the results for ΔN_{it} obtained by CPT with those obtained by SMGT and STMT indicated that stressing had similar effects on border and true interface traps, while the quantitative differences confirmed that the latter two techniques significantly overestimate the density of true interface traps. In addition, different techniques provide information on interface trap densities in different parts of the silicon bandgap. Namely, CPT yields the density of interface traps with energy levels around midgap, SMGT gives the average density of interface traps in the range from the midgap to the energy level of the surface potential corresponding to the threshold voltage, and STMT above that level. Since the energy distribution of interface traps within bandgap is not uniform but is U-shaped [23], the density of interface traps is higher near the bandgap edges (accessible by STMT and SMGT) and lower around the midgap (accessible by CPT). Accessibility of STMT extends further toward the bandgap edges, and that is why this technique yields the highest densities of interface traps.

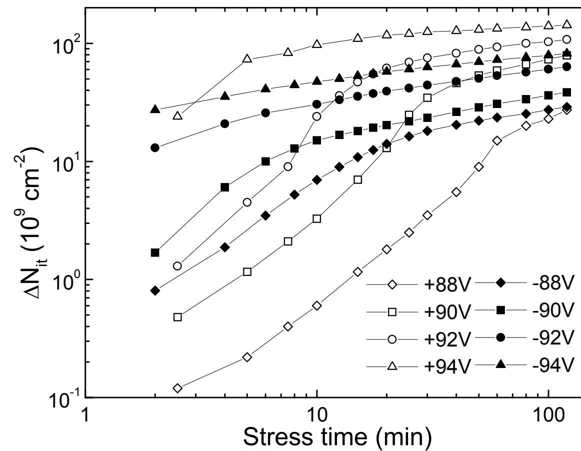


Fig. 4 - *Changes of interface trap density during the electrical stressing of power VDMOSFETs determined by CPT.*

3 Responsible Mechanisms

The mechanisms responsible for the oxide-trapped charge and interface trap buildup are tunnelling processes associated with trivalent silicon $\equiv Si_o^\bullet$ and double donor-like oxygen vacancy $\equiv Si_o^{\bullet\bullet}Si_o\equiv$ defects. Note that the latter defects introduce two trap levels into the oxide bandgap with depths of about 2.4 eV and 6.3 eV [24]. As illustrated in Fig. 5, under the high positive field across the oxide, the electrons can tunnel from silicon conduction band into the oxide conduction band (mechanism 1), and roll down into the gate, representing main contribution to the gate current. Also, the electrons can tun-

nel from $\equiv Si_o^{\bullet}$ and shallower $\equiv Si_o^{\bullet\bullet}Si_o\equiv$ trap levels into the oxide conduction band (mechanism 2), leaving behind positively charged oxide traps ($\equiv Si_o^{+}$ and $\equiv Si_o^{+\bullet}Si_o\equiv$) [9], and also roll down into the gate. Using the procedure given in [14] and data for ΔN_{ot} from Fig. 2 a, the electron tunnelling from neutral oxide traps was shown to be responsible for positive gate oxide-trapped charge buildup, and the barrier height for electron tunnelling (i.e. depth of electron trap levels) was estimated to be about 3.1 eV [11]. This depth of oxide trap levels is in agreement with that of trivalent silicon $\equiv Si_o^{\bullet}$ defects reported in [24]; therefore, the mechanism 2 of oxide-trapped charge buildup is mainly associated with these defects. Using the same procedure and data for ΔN_{it} from Fig. 2 b, it was also shown that the subsequent hole tunnelling from positively charged oxide traps was the mechanism responsible for interface trap buildup, and the barrier height for hole tunnelling was estimated to be about 3.3 eV [11].

The interface-trap levels are distributed around the silicon midgap, which is about 3.8 eV (3.2 + 0.6 eV) below the bottom of oxide conduction band [25]. Having in mind that the electron trap levels are 3.1 eV below the bottom of oxide conduction band, the difference between these trap levels is about 0.7 eV if there is no any local oxide field. Simple calculation shows that, for our stress voltages, oxide traps located around 1.1 nm from interface are at the same energy level as the silicon midgap. It means that holes from these traps can tunnel directly to interface-defect levels associated with interfacial trivalent silicon $\equiv Si_s^{\bullet}$ (mechanism 3), leading to a change of the charge associated with interface traps. On the other hand, holes from traps located deeper in oxide can tunnel directly to interface-defect levels associated with $\equiv Si_s$–H precursors (mechanism 4). This mechanism may cause the release of hydrogen atoms through the dissociation of weak $\equiv Si_s$–H bonds, thus leading to a creation of interface traps ($\equiv Si_s^{\bullet}$ defects) [9]. The estimated depth of interface-defect levels associated with $\equiv Si_s$–H precursors of 6.4 eV (3.1+3.3 eV) is in agreement with finding reported in [26].

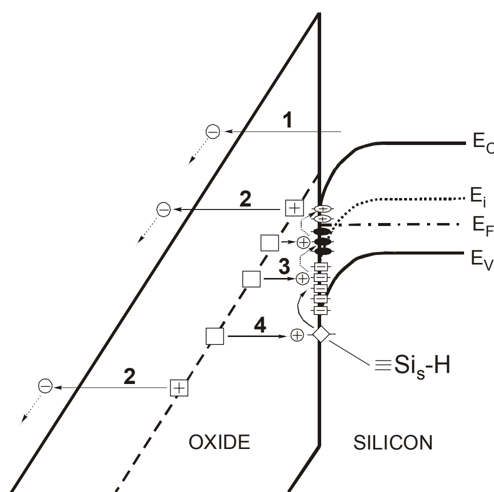


Fig. 5 - *Mechanisms responsible for buildup of oxide-trapped charge and interface traps during the positive gate bias stressing.*

Namely, these levels are distributed at energy levels that are more than 0.5 eV below the top of silicon valence band, i.e. more than 4.9 eV (3.2+1.2+0.5 eV) below the bottom of oxide conduction band. Therefore, the interface trap buildup is mainly due to the mechanism 4. It should be noted that holes and the released hydrogen atoms could form the positive hydrogen ions, which also may cause dissociation of the weak bonds and interface trap creation. As for the oxide traps, by emitting the holes they are neutralized, but are charged again by releasing the electrons into the oxide conduction band (mechanism 2), and the whole process continues.

The above analysis is in line with generally established fact that creation of interface traps is closely linked to oxide-trapped charge, i.e. that the oxide-trapped charge tends to be transformed into the interface traps through a variety of mechanisms [23]. That is the reason why the slope of oxide-trapped charge density changes in log-log scale should be unique, as obtained by STMT (Fig.2 a). Of course, the decrease of oxide-trapped charge due to its transformation into the interface traps does have the influence on its time dependence; i.e. the slope is close to but less than 1 (sublinear dependence) [11]. On the other hand, the interface traps are created with a time delay in respect to oxide-trapped charge, and a certain “threshold” oxide-trapped charge (which would increase the local electric field enough to create narrower barrier for hole tunnelling) is required before any significant creation of interface traps can start. Once this threshold is reached, the rate of interface trap increase becomes much higher than that of oxide-trapped charge with a slope larger than 1 [11] (superlinear dependence, also observed in irradiated devices [23]). Charge associated with the increase of interface traps compensates the local oxide field, which leads to a significant decrease of its slope at the stress time approximately corresponding to the threshold voltage rebound, which also can be seen in Fig.2 a. The additional reason for the slope decrease may be a gradual decrease in concentration of defects available for interface trap creation.

The above analysis is also in accordance with observed evolution of gate current during the stressing shown in Fig.6. Namely, the initial rapid current increase is a consequence of the narrowing of barrier for electron tunnelling (mechanism 1) due to the increase of local electric field associated with positive oxide charge buildup. After the threshold oxide-trapped charge is reached and creation of interface traps becomes significant, the current starts decreasing as a consequence of the barrier widening due to local field compensation.

Note that similar gate current evolution has been also reported by Picard et al. [6] and Schwalke et al. [7], but they have explained the appearance of current peaks in terms of Fowler-Nordheim tunnelling and related mechanisms; i.e. the increase of gate current by hole trapping and its decrease by electron trapping. Yet, Schwalke et al. have admitted that the observed positive oxide-trapped charge buildup was larger than expected from Fowler-Nordheim injection, suggesting that an additional charge-generation was present.

As illustrated in Fig.7, under the high negative electric field across the oxide, the holes can tunnel from the silicon valence band to the deeper $\equiv Si_o^{\bullet\bullet} Si_o \equiv$ trap levels (mechanism 1), thus leading to a positive gate oxide-trapped charge buildup. Using the procedure given in [14] and results shown in Fig.2 a, the barrier height for hole tunnelling was estimated to be about 2.1 eV [13], yielding the depth of oxide-trap levels of

about 6.5 eV (3.2+1.2+2.1 eV), which was in good agreement with values reported in [24, 27].

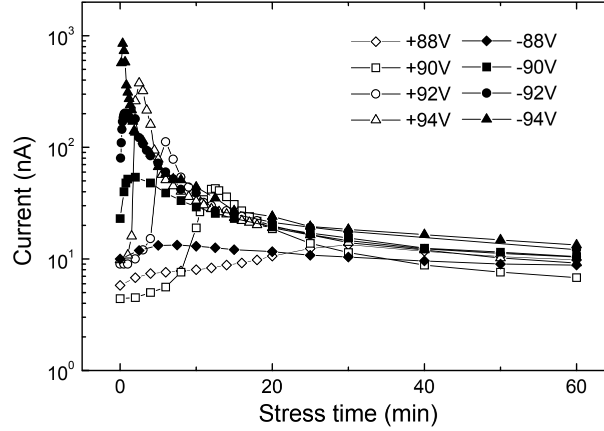
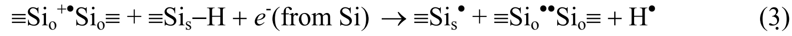


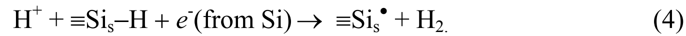
Fig. 6 - *Evolution of gate current during the stressing of power VDMOSFETs.*

The interface trap buildup is a consequence of oxide-trapped charge transformation into the interface traps, and can be explained through the electro-chemical reaction between interfacial precursors $\equiv Si_s{-}H$ and positive oxide-trapped charge already built-up near the interface [9]:



$$\equiv Si_o^{+\bullet}Si_o\equiv + \equiv Si_s{-}H + e^-(\text{from Si}) \rightarrow \equiv Si_s^{\bullet} + \equiv Si_o^{\bullet\bullet}Si_o\equiv + H^{\bullet} \quad (3)$$

This mechanism causes the release of hydrogen atoms through the dissociation of weak $\equiv Si_s{-}H$ bonds, thus leading to a creation of interface traps associated with trivalent silicon defects $\equiv Si_s^{\bullet}$. Note that released hydrogen atoms and tunnelling holes can form positive hydrogen ions, which also may cause dissociation of weak $\equiv Si_s{-}H$ bonds, also leading to interface trap creation through the following electro-chemical reaction [4]:



$$H^+ + \equiv Si_s{-}H + e^-(\text{from Si}) \rightarrow \equiv Si_s^{\bullet} + H_2 \quad (4)$$

Under the high negative field across the oxide, electrons can tunnel from poly-silicon conduction band into the oxide conduction band (mechanism 2), and roll down into the silicon, representing main contribution to the gate current. As can be seen in Fig. 6, qualitatively the same gate current evolution is observed as in the case of positive gate bias stressing. However, negative gate bias causes higher gate current (because of higher field due to a smaller voltage drop on silicon) and its more rapid initial increase (because of more rapid initial buildup of oxide-trapped charge). Note that in the case of negative bias stressing, the initial rapid current increase is a consequence of the narrowing of barrier for electron tunnelling due to decrease of local electric field in the vicinity of oxide-silicon interface associated with buildup of positive oxide-trapped charge. On the other hand, gate current decrease may be a consequence of barrier widening due to decrease of local electric field near the polysilicon-oxide interface associated with electron trapping at amphoteric silicon vacancy defects [24] (mechanism 3).

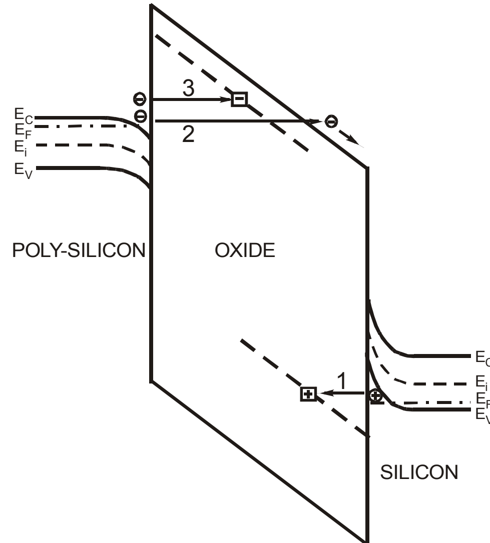


Fig. 7 - *Mechanisms responsible for buildup of oxide-trapped charge and interface traps during the negative gate bias stressing*

4 Conclusion

We have shown that gate bias stressing caused significant threshold voltage shift and mobility degradation in power VDMOSFETs. The negative bias stressing caused more rapid initial changes of both threshold voltage and mobility, but the final threshold voltage shift and mobility reduction were significantly smaller than in devices stressed by positive gate bias. The underlying changes of positive oxide-trapped charge and interface trap densities were calculated and analysed in terms of the mechanisms responsible.

In the case of positive bias stressing, the electron tunnelling from neutral oxide traps associated with trivalent silicon $\equiv Si_o^{\bullet}$ defects into the oxide conduction band was shown to be mainly responsible for positive oxide-trapped charge buildup. The subsequent hole tunnelling from these positively charged oxide traps ($\equiv Si_o^{+}$) to interface-defect levels associated with $\equiv Si_s–H$ precursors was shown to be mainly responsible for interface trap buildup. The depths of oxide trap and interface-defect levels were estimated to be 3.1 and 6.4 eV, respectively, which was in good agreement with the values reported in [24, 26].

In the case of negative bias stressing, hole tunnelling from the silicon valence band to oxygen vacancy defects $\equiv Si_o^{\bullet\bullet}Si_o\equiv$ was shown to be responsible for positive oxide-trapped charge buildup. The depth of oxide-trap levels was estimated to be 6.5 eV, which was in good agreement with values reported in [24, 27]. On the other hand, interface trap buildup was explained through electro-chemical reactions of positive oxide-trapped charge built-up near the interface and hydrogen ions with interfacial precursors $\equiv Si_s–H$.

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