

Second-Order Sigma-Delta Modulator in Standard CMOS Technology

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Abstract: As a part of wider project sigma-delta modulator was designed. It represents an A/D part of a power meter IC. Requirements imposed were: SNDR and dynamic range > 50 dB for maximum input swing of 250 mV differential at 50 Hz. Oversampling ratio is 128 with clock frequency of 524288 Hz which gives bandwidth of 2048 Hz. Circuit is designed in 3.3 V supply standard CMOS 0.35 μm technology.

Keywords: Analog-to-digital conversion, Sigma-delta modulation

1 Introduction

The use of oversampling sigma-delta modulators in the integration of high-resolution analog-to-digital converters has shown promise for overcoming the analog component limitations inherent in modern VLSI technologies. Sigma-delta modulators employ coarse quantization enclosed in one or more feedback loops. By sampling at a frequency that is much greater than the signal bandwidth, it is possible for the feedback loops to shape the quantization noise so that most of the noise power is shifted out of the signal band. The out of band noise can then be attenuated with a digital filter. The degree to which the quantization noise can be attenuated depends on the order of the noise shaping and the oversampling ratio.

In addition to their tolerance for circuit nonidealities, oversampled A/D converters simplify system integration by reducing the burden on the supporting analog circuitry. Because they sample the analog input signal at well above the Nyquist rate, precision sample-and-hold circuitry is unnecessary. Also, the burden of analog antialiasing filter is considerably reduced. Much of its function is transferred to the digital decimation filter, which can be designated and manufactured to precise specifications, including a linear phase characteristic.

To fulfil the requirements we chose the second-order modulator. In theory the first-order modulator is sufficient [1], but the second-order will give enough margins for circuit non-idealities and process variations.

This paper is organized as follows: Sections 2 and 3 describe implementation of the modulator architecture. In section 4 a method for behavioral simulation of architecture implementation is presented. Finally, section 5 describes the design of the proposed second-order modulator.

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2 Modulator Design

The modulator architecture is implemented by combining two summing integrators with comparator and 1-b D/A converter, as shown in Fig. 1 [2]. The most important building block in this architecture is a summing integrator, for which the output w is the delayed integration of a weighted sum of inputs v_m . In the time domain, the output is

$$w((n+1)Ts) = w(nTs) + \sum_m a_m v_m(nTs), \quad (1)$$

where Ts is the modulator's sampling period. The z transform of the output is

$$W(z) = \frac{z^{-1}}{1-z^{-1}} \sum_m a_m V_m(z), \quad (2)$$

where $V_m(z)$ is the z transform of $v_m(nTs)$.

The remaining building blocks in the analogy portion of the modulator are comparator and 1-b D/A converter. The comparator circuit acts as a 1-b A/D converter that map its input into one of two digital output codes. The two digital output codes are then mapped back into analog levels by the D/A converter. If the two output codes of the comparator are defined as $\pm 1/2$, then the D/A converter, neglecting D/A errors, can be represented simply by gain block.

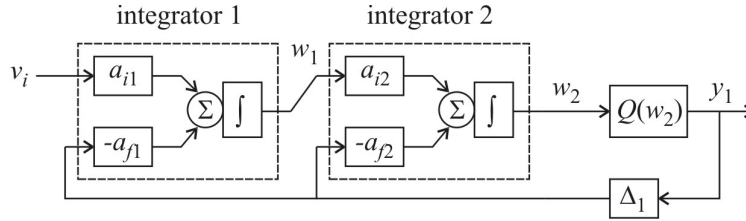


Fig. 1 - Modulator architecture implementation.

3 The Integrator Architecture

Integrators are implemented as the switched-capacitor circuit. Two main sources of noise in switched-capacitor integrator are: thermal noise from the amplifier and switches, and flicker noise from the amplifier. The thermal noise from switches (kT/C noise) is limited by using sufficiently large capacitors to restrict the noise bandwidth. Minimum value used for capacitors in first integrator is 5 pF (CREF). The flicker noise is attenuated using the correlated double sampling topology shown in Fig. 2 [3].

In the double sampling integrator, a nonoverlapping two-phase clock is used. Switches $C1$ and $C1A$ conduct during first clock phase, and switches $C2$ and $C2A$ conduct during the second clock phase. Switches $C1A$ and $C2A$ are opened slightly ahead of switches $C1$ and $C2$ respectively to reduce signal-dependant charge injection onto sampling capacitors C_S [4]. During the first phase, the input V_{in} is sampled across

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C_S while amplifier offset is sampled on C_{CDS} . In the second clock phase a charge proportional to the input voltage V_{in} minus feedback voltage V_{ref} is transferred from C_S and C_{ref} to C_F , while dc offset and flicker noise of the amplifier are cancelled by the voltage stored on C_{CDS} . For proper operation, C_{CDS} must be much larger than input capacitance of the amplifier. In this design C_{CDS} is chosen to be 5 pF.

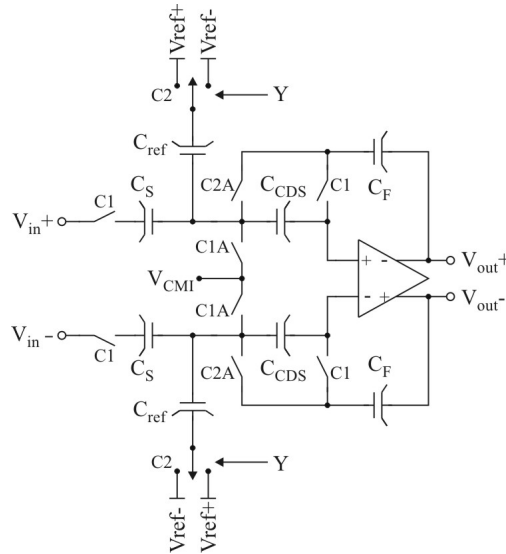


Fig. 2 - Correlated double sampling integrator.

Table 1

Integrator gain values

Gain	Value
a_{i1}	1.0
a_{f1}	0.2
a_{i2}	0.5
a_{f2}	0.25

Values for integrators' gain determine the signal swing at the output of each integrator. To protect integrators from saturation the proper integrator gain must be used, but still being practical to implement. The integrators' gains used in this design are summarized in Table 1 [5].

4 Behavioral Simulation

Verification of the architecture implementation from Fig. 1 is done using *Matlab Simulink* environment [6]. Ideal modulator output spectrum for a sinusoidal input signal of 50 Hz and amplitude of 125mV is shown in Fig. 3.

The analog circuit block cannot precisely perform their ideal function, so most of modulator nonidealities must be taken into account. Such are sampling jitter, kT/C noise, and operational amplifier parameters (white noise, finite dc gain, finite bandwidth, slew rate and saturation voltages). Only the first integrator needs to be simulated with nonidealities, since noise shaping does not attenuate their effects.

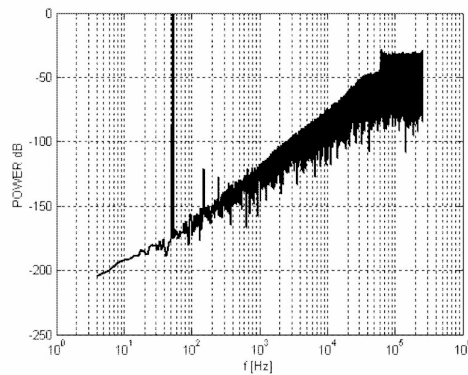


Fig. 3 - Ideal modulator's output spectrum.

Simulink model used to simulate nonidealities is shown in Fig. 4 [7]. Table II gives values for modulator parameters used in the simulation. Only white noise is considered, while flicker noise and dc offset are neglected, because the first integrator has correlated double sampling. Output spectrum obtained from simulation data for the sinusoidal input signal of 50 Hz and amplitude of 125mV of the modulator with modelled nonidealities is shown in Fig. 5.

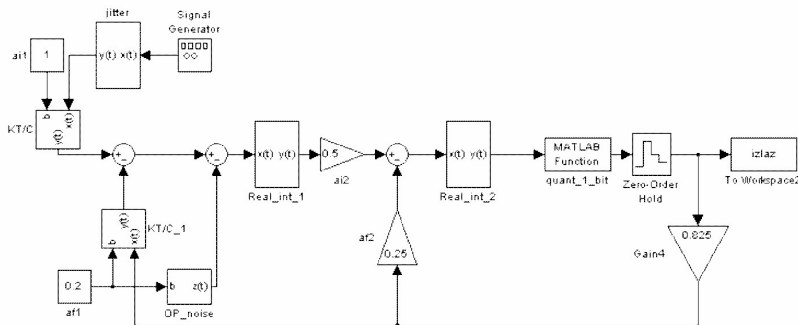


Fig. 4 - Simulink model.

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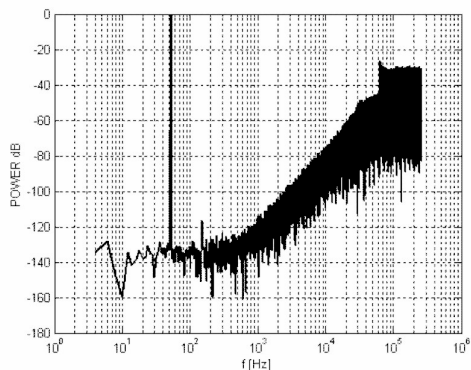


Fig. 5 - Output spectrum with nonidealities.

Table 2

Modulator nonidealities.

Modulator parameter	Value
Sampling jitter	20 ns
Switches (kT/C_S) noise	25 pF
Input-referred operational amplifier noise (thermal)	$70 \mu\text{V}_{\text{rms}}$
Finite dc gain	10^3
GBW	2.5 MHz
Slew-rate	4 V/ μs

5 Circuit design

After behavioral level simulations were performed we had enough parameters for transistor level implementation. All required analog blocks (operational amplifiers, bandgap reference, switches, capacitors and quantizer) were designed, simulated, and then layout is carried out.

The sigma-delta modulator depicted in Fig. 1 was designed for fabrication in 0.35- μm CMOS technology. The operational amplifier used in integrators is the most critical element of the modulator. Behavioral simulation with nonidealities indicates that a slew rate of 4 V/ μs , GBW of 2.5 MHz is sufficient to meet performance objectives. Since the comparator can be designed to be quite fast, the settling speed of the integrator ultimately limits the achievable sampling rate of the modulator, even if complete settling is not required. The need for high speed, coupled with a relatively modest gain requirement of 60 dB to suppress harmonic distortion, encouraged the use of the folded-cascode operational amplifier [8].

Figure 6 shows fully differential folded-cascode operational amplifier used in this design. The common-mode levels in the fully differentially amplifier are set by the

common-mode feedback (CMFB) circuit shown in Fig. 7. Bias voltages are provided by a wide-swing cascode current mirror bias circuit.

The second major component of the modulator is the comparator. The performance of the modulator is relatively insensitive to comparator offset and hysteresis since the effects of those impairments is attenuated by the second order noise shaping. The regenerative latch has been used to implement the comparator [2].

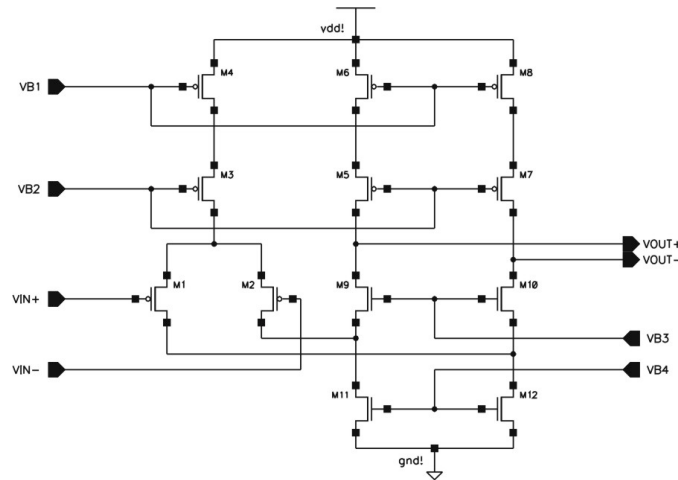


Fig. 6 - Folded cascode op-amp.

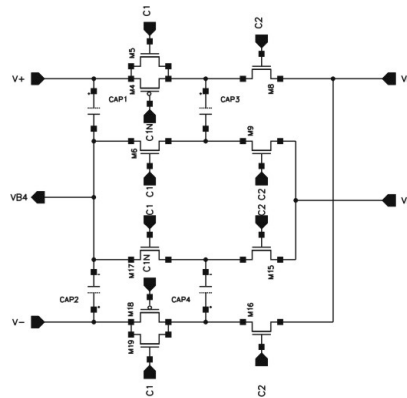


Fig. 7 - CMFB circuit.

Output spectrum obtained from transistor level simulations data for 8 kHz 125mV sinusoidal input signal is shown in Fig. 8. Input signal frequency is 8 kHz, which is enough to have a reasonable simulation time, while giving enough samples (16 k samples) to perform a FFT.

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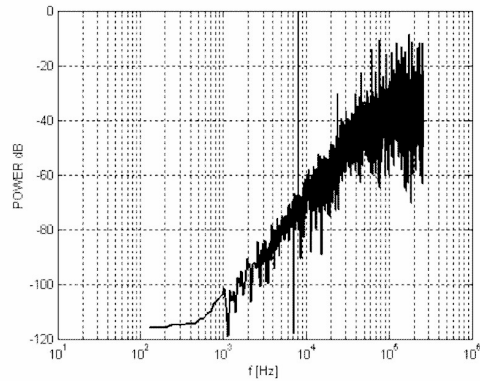


Fig. 8 - Output spectrum from transistor level simulation.

During layout implementation a special attention was paid to matching and noise considerations. In Fig. 9 the layout of the modulator is shown. Modulator occupies the area of 0.57 mm².

6 Conclusion

In this paper, a second-order sigma-delta modulator design has been described. Transistor level simulation results show that the designed circuit fulfils the imposed requirements. Modulator is designed using Cadence Design System [9] and AMI Semiconductors CMOS 0.35 μm (C035-2P5M-AS) technology. Currently chip is in the fabrication phase.

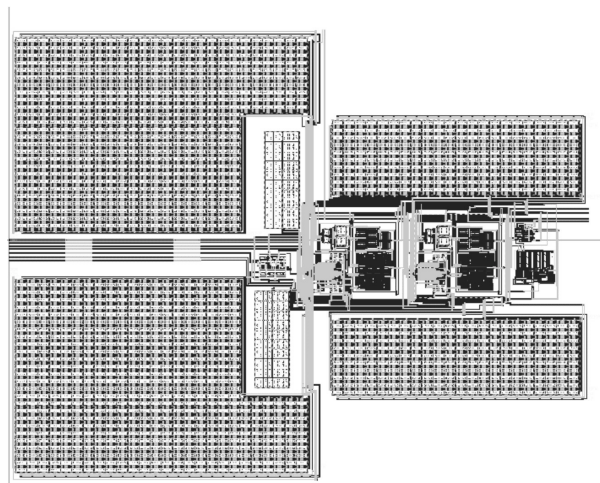


Fig. 9 - Layout of the modulator.

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